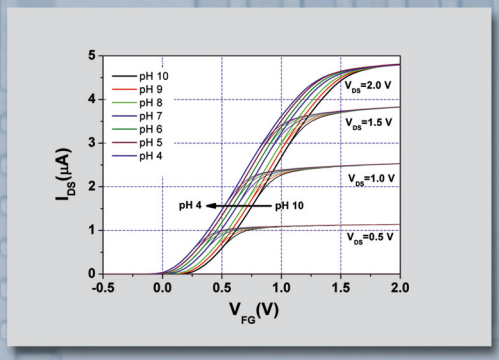

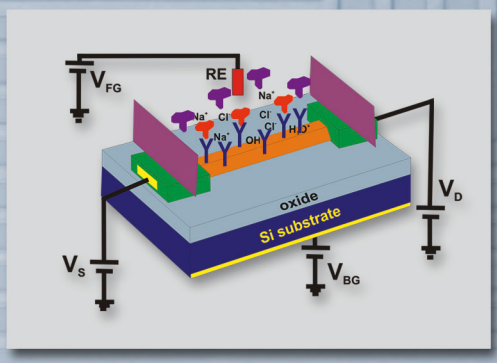

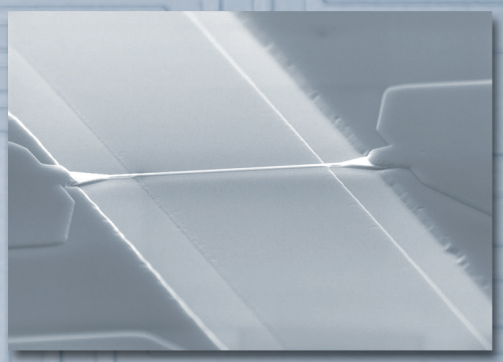

Silicon nanowire transistor arrays for biomolecular detection

Xuan Thang Vu

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Dedicated to my wife and my daughters

Abstract

Biosensors based on nano-scale electronic devices have the potential to achieve exquisite sensitivity for the direct detection of biomolecular interactions. Silicon nanowire field-effect transistor (SiNW-FET) is the most promising candidates for these purposes because of their biocompatibility, very high surface-to-volume ratio, fast response, and good reliability of the signal. In the last few years, several promising results based on SiNW sensors, which were either fabricated by “top-down” or “bottom-up” methods, have been reported, such as biosensors for protein binding, DNA hybridization or the detection of extracellular signals from electrogenic cell.

The aim of this work was to fabricate SiNW arrays in a large scale with robust methods and then apply for the detection of biomolecules. To achieve these tasks, we have developed a novel “top-down” approach for wafer-scale processes of SiNW arrays based on a combination of two technologies: the novel and high throughput nanoimprint lithography and wet anisotropic etching of silicon. Devices were fabricated at the clean room facility at the Institute of Bio- and Nanosystems (IBN), Research Center Juelich, Germany. By our approach, the dimensions of the SiNWs can simply be tuned using different etching times of the sub-processes. This process offers a large dimension control of the desired nanowire structures without using an expensive mask or highly complicated nanostructuring of the devices. For the full fabrication process, we employed thermal nanoimprint lithography and anisotropic etching of Si by tetramethylammonium hydroxide (TMAH) in combination with other micro-fabrication techniques such as wet etching, dry etching and photolithography to create the SiNW array sensors. Two complete fabrication rounds were finalized including top-down structuring, implantation and silicidation of contact lines, passivation of the devices with a high quality SiO_2 layer deposited by a “low pressure chemical vapor deposition” (LPCVD) process to enable device operation in liquid environments, gate oxide formation, metallization. Finally, chips were wire bonded and encapsulated with epoxy glue enabling stable and reliable operation within electrolyte environments. Main advantages of our fabrication protocol are that the sensors could achieve high sensitivity, while possible mass production and reproducibility of the devices are guaranteed. The chip designs were based on either 4×4 arrays for the first round or 28×2 arrays for the second round

The SiNWs were thoroughly electronically characterized by using different configurations such as back gate control (V_{BG}) or front gate control (V_{FG}). We also studied the difference between front-gate and back-gate operation of the devices with respect to the stability of the electric signal.

The SiNW sensors were then further applied for the detection of chemical and biological substances. First, we demonstrated the pH sensitivity of the devices and found that with front-gate operation, the pH sensitivity of the devices was 41 mV/pH and did not depend on the wire dimensions. In further experiments the devices were used for detection of Ca^{2+} ions and for monitoring the buildup of polyelectrolyte multilayer as a model to understand the sensitivity and detection mechanism of the SiNWs. It was also demonstrated that the SiNW arrays were sensitive to biotin-streptavidin binding and DNA immobilization and hybridization. The SiNW sensors generally showed approximately 8 times larger signals for biomolecular detection in term of flat-band voltage change in comparison to past experiments with our standard microscale ISFETs reported previously.

Zusammenfassung

Nano-Scale Biosensoren haben das Potential hervorragender Sensitivität für die direkte Detektion von Biomolekül Interaktionen. Aufgrund der guten Biokompatibilität, dem hohen Oberflächen zu Volumen Verhältnis, der schnellen Antwortzeit und der guten Zuverlässigkeit sind die sogenannten Silizium Nanowire Feldeffekt Transistoren (SiNW-FETs) von allen Ansätzen die vielversprechendsten Kandidaten. In den letzten Jahren wurde über verschiedene vielversprechende Ergebnisse basierend auf SiNWs zur DNA Hybridisierung oder zur extrazellulären Detektion von Aktionspotentialen berichtet. Die Fabrikation erfolgte entweder durch "top down" oder "bottom up" Methoden.

Ziel dieser Arbeit war die Erstellung einer Methode zur Fabrikation eines großen Arrays von SiNWs auf einem Chip für die Anwendung in der Biosensorik.

Um dieses Ziel zu erreichen wurde ein neuer "top down" Ansatz entwickelt, der die Prozessierung ganzer Wafer ermöglichte und auf der Kombination der neuartigen Nanoimprint Lithographie mit hohem Durchsatz und anisotropem Ätzen von Silizium basiert. Die Chips wurden vollständig im Institut für Bio und Nanosysteme des Forschungszentrums Jülich gefertigt. Im gesamten Fabrikationsprozess kamen neben der nanoimprint Lithographie und dem anisotropen Ätzen mittels TMAH noch weitere Mikrofabrikationsschritte, wie nasschemisches Ätzen, Trockenätzen oder Photolithographie zum Einsatz.

Das Chip Design bestand entweder aus einer 4x4 Matrix, oder einer 28x2 Matrix. Durch den hier entwickelten Ansatz können die Dimensionen der Drähte, durch die Verwendung unterschiedlicher Ätzzeiten, einfach modifiziert und angepasst werden. Dies ermöglicht die volle Kontrolle der Drahtgrößen, bei gleichzeitig minimalen Kosten, da keine zusätzlichen Masken oder komplizierten Nanostrukturierungen verwendet werden müssen.

Weiterhin erfolgt noch die Passivierung der Leiterbahnen mit einem hochqualitativen SiO_2. Hierzu wurde die SiO_2 Schicht mittels "low pressure chemical vapor deposition" (LPCVD) abgeschieden.

Den letzten Schritt stellen das Drahtbonden der Chips und die Verkapselung mittels Epoxy-Kleber dar. Dies führte zu einem stabilen Chip der in Elektrolyt Umgebung betrieben werden kann.

Hauptvorteil unseres Fabrikationsprotokolls ist die Möglichkeit der Massenproduktion mit guter Reproduzierbarkeit in Kombination mit der hohen Sensitivität der Sensoren.

Die Nanodrähte wurden sorgfältig mittels verschiedener Konfigurationen wie “front gate“ und „back gate“ Kontaktierung charakterisiert und die Unterschiede in Bezug auf Stabilität des elektrischen Signals analysiert.

Die Demonstration der Leistung der Chips erfolgte auch anhand der Detektion chemischer und biologischer Signale. Mit der „front gate“ Konfiguration wurde eine pH Sensitivität von 41 mV/pH gemessen, die unabhängig von den Drahtdimensionen war. In weiteren Experimenten kamen die Chips zur Detektion von Ca^{2+} Ionen und zum online Monitoren des Aufbaus von Polyelektrolyt Stapeln zum Einsatz. Dies wurde zur Erstellung eines Funktionsmodells zur Analyse der hohen Sensitivität der Drähte verwendet. Schließlich konnte noch die Bindung von Biotin-Streptavidin sowie die Immobilisierung und Hybridisierung von DNA mittels des Chips verfolgt werden.

Die hier produzierten SiNWs zeigten ein viel größeres Signal bei der Detektion von DNA als es in vergangenen Experimenten mit Standard micro-ISFETS berichtet wurde.

Contents

Chapter 1. Introduction

Sensing of chemical and biological substances has an important role in modern life. This is due to the fact that many commonly used chemical and biological substances are dangers to human health, agriculture and environment. Highly sensitive and selective detection of these substances offer many applications in various fields such as security [1], clinical screening and diagnosis [2, 3-5], drug discovery, food control, and environmental monitoring [4, 6-8], and also help for understanding of the biological systems [9, 10]. In this sense, it is imperative to develop a sensor for these purposes. In doing so, the sensor needs to meet some basic requirements, such as fast response, be small, robustness, be relatively cheap in terms of fabrication, present stability over long periods and be specific to one analyte or at least to a group of analytes of interest. To fulfill these tasks, most of the time interdisciplinary solutions including physics, electronics, chemistry, and biochemistry need to be developed for those sensors.

In this context, biosensors are the devices of choice, ideally small and portable, that allow the selective quantization of chemical and biochemical analytes. They consist of two main components: A transducer and a (bio)chemical recognition element. The (bio)chemical recognition element is accomplished by exploiting the natural selectivity of biochemical processes, in which enzymes, antibodies, chemo receptors, and nucleic acids meet their respective binding partner with high affinity. In the presence of analytes, the specific

binding events of the biological systems at the surface of the transducer cause a change in local environment at the surface. The transducer monitors the effect, and converts the biochemical recognition event into a measurable signal. Transducers may measure gravimetric, optical, thermal, or electrochemical effects that change during the binding process. In some concepts, the analyte of interest is coupled to a reporter molecule – the so-called label – and the effect is caused by this label interacting with the recognition site. Because of the many reasons, like, to avoid an extra binding step of the label to the analyte, to reduce the consumption of label material and the cost, and finally, to enhance the overall assay time, there is nowadays a strong drive towards the development of label-free biosensors. The principal of the label-free biochemical sensor is illustrated in figure 1.1. In this concept, receptor molecules are immobilized on the transducer surface and the binding event of the sample molecules to the receptor create change in electric signal of transducer such as a change in monitoring current or voltage. The signal changes are amplified and measured by electronic equipment and the data are stored. In the last step, data analysis and some calculations give final results. There are many potential advantages to label-free approaches, most noteworthy is that they can provide direct monitoring of analyte binding to target molecules without modifying the molecules of interest with labels or by using reporter systems.

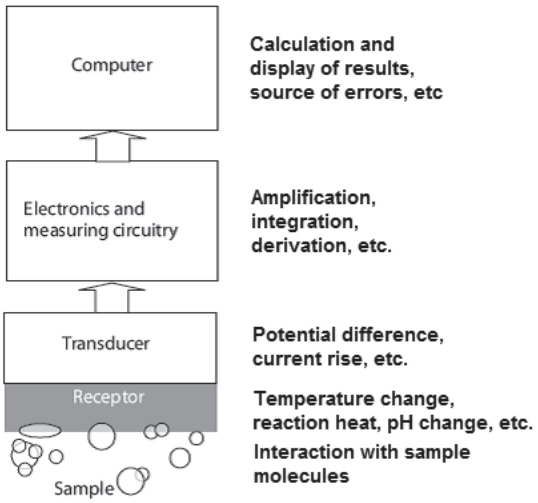

Figure 1.1 *Scheme of a typical biochemical sensor [11]. The transducer converts the biochemical signal on the surface of the transducer to the readable electronic signal. The signal is then amplified and displayed by electronic readout.*

*****

Nowadays, exploration of nanomaterials and nanotechnology for different biomedical applications has been highly investigated. For example, the nanotechnology is enabling the development of small, inexpensive and highly efficient and sensitive biosensors, with broad applications [12-14]. It is envisaged that by enhancing the interactions that occur at the nanoscale, sensors may offer significant advantages like enhancing the sensitivity and selectivity over conventional sensors. Such advantages are special due to the similarities in sizes between the nanoscaled sensors and those detectable molecules. These unique properties of nanoscale materials make them ideal candidates for sensing applications. The devices could either be integrated into existing micro technology platform or creating new and independent platforms [15, 16]. Using nanotechnology processes, the sensor devices can be highly integrated enabling a broad range of applications such as multiplexing detection. In this case, various specific probe molecules are immobilized on each sensor of a large scale array and specifically bound to a target contained inside an analyte solution such as blood serum.

Improving sensitivity is a major issue while developing nanoscale sensor devices. At the nanoscale, sensors should be able to detect a single molecule or atom [17-21]. The small size, light weight, and high surface to volume ratio of nanostructures make them ideal candidates for the detection of chemical or biological species with remarkable sensitivities that were initially thought to be unattainable. In addition, in nanostructure the entire structure can be affected by the analyte and not only the surface as the conventional sensors [12]. Another aspect of nanoscale devices is the fast response time of such sensors. In this case, the speed, in which species can be detected, is most definitely affected by the sensor dimensions [22]. Hence, nanoscale sensors present opportunity of improving the sensor's dynamic performance, which is another key objective of nanosensor devices.

A wide range of nanomaterials and nanoscale devices are promising candidates for biosensing applications [13, 23-25]. For instance, nanoparticles or quantum dot offer to tune or to amplify the response of standard optical sensors towards narrower frequency bands to increase the accuracy and selectivity of such sensors and enable medical imaging of different targets [18, 23, 25-27]. The surface of nanoparticles can be functionalized with different species such as proteins or DNA for specific applications [25, 28, 29]. Nanocantilever sensors can measure the deflection of a laser beam or a piezoresistive element upon binding of desired molecules to a thin cantilever [30-32]. Each of these methods offers promising performances, however, there are also coherent limitations of such approaches because of the mandatory laboratory readout.

*****

Since the introduction of ion-selective field-effect transistor (ISFET) [33], the device was extensively studied as prospective biosensor to detect all kinds of biomolecules. The ISFET structure is derived from a metal-oxide-semiconductor field-effect transistor (MOSFET), a basic electronic element in all of the modern electronic devices. In ISFET, the metal gate contact of the MOSFET is removed and the gate dielectric material is directly employed as a transducer for detection of chemical and biological substances. Normal ISFET has the gate length from few μm to few hundreds of μm. The progress in the detection of variety of biomolecular interactions using ISFETs with either potentiometric or impedimetric principles are reported in literatures [34-48]. The details of ISFET device and the two different methods will be discussed in chapter 2 of this thesis.

Scaling of the microscaled ISFET device to nanoscaled device for biosensing applications by using a silicon nanowire (SiNW) was firstly demonstrated by C. Lieber and coworkers [49]. After the pioneering work, there are extremely increase of researches on SiNW sensors for bioelectronics applications. SiNW has potential to produce an ultrahigh sensitive, label-free sensor for a broad range of applications. At the nanoscale, the SiNW structure increases the surface-to-volume ratio, the geometry of the SiNW restricts current flow to a much smaller confined region than in usual Si bulk ISFET devices and thus is increasing the device sensitivity such that only a small number of charged molecules can cause a measurable signal. By modifying the surface of the SiNWs with different type of catcher molecules such as antibodies, aptamers, single stranded DNA or PNA, specific proteins, or other molecules, the device is very sensitive to detect many different target analytes, enabling varieties of different biomedical applications [49-65]. Beside the chemical or biomolecular detections, the SiNW devices can also be used to study the activity of electrogenic cells [10, 66, 67] or even the signal propagation and communication inside neuronal networks [10].

In the related biosensors and bioelectronics literatures, several different methods for SiNW fabrication are described [49, 53, 54, 61, 68-73]. They can be divided into two categories: a “bottom up” approach that is usually based on vapor-liquid-solid method (VLS) with metal precursors (mostly Au), and a “top down” approach that is based on advanced lithography techniques. In the latter case usually silicon-on-insulator (SOI) substrates were used and mostly electron-beam lithography (EBL) is used to define structures. In the “bottom up” approach epitaxial, cylindrical nanowires with a diameter from several nm to 100 nm are grown with high quality. However, this approach has several limitations such as complex

chip integration, difficulties in individual nanowires positioning, and a difficult process to achieve reliable *ohmic* contacts [72]. These result in a low yield of working devices per fabrication process which leads to immense fabrication costs per device and prevent commercial products so far. In contrast to this, the "top down" approach has several advantages. First of all, the nanowires are uniform in size and well aligned as a 'process intrinsic' results. The "top down" methods usually produce functional nanowires in high yields, and in predetermined orientation and position on the substrate. In addition the device fabrication can be adapted to industrial CMOS processes, promising a low-cost production of single use test kits.

The nanowires produced by the "top down" approach typically have widths from 50 nm to few hundreds of nm and lengths ranging from 3 μm up to 1 mm [54, 61, 70, 71, 74, 75]. However, realizing nanowires in very small diameters is one of the big challenges of the "top down" approach, since EBL has its limitation as well as it is a low through put technology. Deep UV lithography would in principle fulfill the requirements, but is difficult to access at the research level. Several strategies of size reduction for SiNWs fabricated in a "top down" approach can be realized by a process called "self-limiting oxidation" after structuring [54, 68, 76] or by wet anisotropic etching of Si [61, 75]. By these approaches, the size of the SiNW can be achieved in the same range as in the "bottom up" approach. In addition, the sensitivity of the devices fabricated by the "top-down" approach depends on its fabrication protocol. One major problem of the direct "top down" approach is that the SiNWs are usually defined by a reactive ion etching (RIE) process. It was previously described that in this case uncontrolled plasma reactions create defects on the SiNWs surface [77-79] led to degradation of the electronic properties, and hence, decreased sensitivity of the devices [61, 80]. In contrast to this, SiNWs fabricated by wet anisotropic etching of Si with e.g. tetramethylammonium hydroxide (TMAH) showed high electric performances [80] as well as improved sensitivity of the finalized SiNW sensors [61].

*****

The goal of this thesis was to create SiNW-FET arrays by "top-down" approach on wafer–scale level for biosensors and bioelectronics applications. To achieve our targets, three steps were conducted: i) first, fabrication of robust and high quality SiNW-FET arrays, ii) second, electronic and electrochemical characterization of these devices and developing an amplifier readout for the SiNW chips, iii) demonstrating the devices as label-free biosensor

for the detection of chemical and biological species such as DNA hybridization, or protein interactions. All the experimental results are presented in four chapters in this thesis.

The fundamental aspects of this work are covered by chapter 2. Section 2.1 will discuss the general principle of field-effect transistor operation as biosensors and the related theories for signal modeling. Section 2.2 will give an overview about related SiNWs' works reported in literature as ultra-sensitive biosensors as well as described advantages of these devices over traditional micro scale ISFETs and theoretical considerations for such devices. Section 2.3 will give an overview about the novel nanoimprint lithography techniques and the anisotropic wet etching of Si by TMAH solution.

Chapter 3 will present and discuss in details all experimental protocols that have been used throughout this work. In the first part of this chapter, the sensor designs and the fabrication process flows are shown in detail as well as the critical points in the fabrication process are addressed. The next parts provide details about the measurement setups, SiNW characterization procedures and the experiment protocols for pH sensing, the detections of multilayer polyelectrolytes build up, Ca^{2+} ion binding to oligopeptides, biotin-streptavidin binding and DNA immobilization and hybridization by the SiNW devices.

Chapter 4 will present and discuss about the results of SiNW arrays fabrication and characterization. The results of the chip fabrication process will be presented and discussed in the first part of this chapter (section 4.1). In section 4.2, the electronic characterization results of the devices will be discussed in detail. Section 4.3 gives some remarks of the chip fabrication and characterization.

In chapter 5, the results of the biomolecular detection using the SiNW arrays such as the pH sensitivity experiments of the nanowires, highly sensitive detection of Ca^{2+} ion, electronic monitoring during the layer-by-layer adsorption of polyelectrolyte, biotin-streptavidin molecules binding as well as for the detection of DNA molecules are presented and discussed.

Chapter 6 will conclude this thesis and give outlook for future improvements and applications of the system.

Chapter 2. Fundamentals

2.1. The ISFET as label-free biosensors

This section gives a short introduction about the working principle of an ISFET device and the basic principle of the device operation for biosensor applications.

2.1.1. ISFET: structure, operation and characteristics

Structure

The ion-sensitive field-effect transistor (ISFET) was invented by P. Bergveld in 1970 [33]. The device was derived from the metal-oxide-semiconductor field-effect transistor (MOSFET), a basic device in microelectronic circuits. Both devices have identical structures except for the gate electrode that contacts the gate oxide. For instance, while the MOSFET employs a metal or polysilicon layer as a gate electrode [83, 84], the ISFET employs a system of reference electrode immersed in the electrolyte solution as a gate electrode.

The ISFET device generally consists of four terminals: source, drain, bulk and gate electrodes. In a normal operation mode, the bulk terminal is set to the same voltage as the source terminal, normally grounded. Simply, the ISFET has three terminals: source, drain and gate electrodes. A schematic of a p-channel ISFET device is illustrated in figure 2.1.

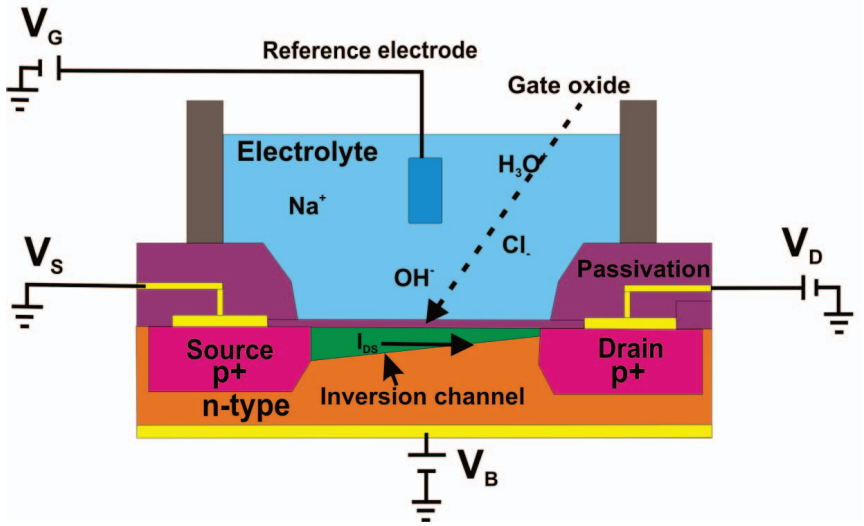

Figure 2.1. *Schematic illustrates cross-section of a p-channel ISFET device. Source and drain terminals are defined by the p^+ regions in an n-type silicon substrate. Gate capacitor is a thin layer of oxide that separates the Si substrate from electrolyte solution. The gate voltage is applied through a reference electrode immersed in electrolyte solution on top of the gate oxide. The thick passivation layer on the contact lines is necessary for a reliable operation of the devices in the different electrolyte solution as well as to avoid interfering with the signal at the gate oxide.*

The source and drain regions (*p^+ regions*) are highly doped by acceptor ions in the *n-type* Si substrate and, thus, create a *pnp*- structure inside the substrate. A thin layer of oxide, called *gate oxide*, is grown on top of the *n-type* silicon substrate between source and drain, acting as a capacitor for the field effect. In order to limit the capacitive coupling of the source and drain contact lines and to avoid leakage current into the signal of the ISFET, the source and drain contact lines are covered by a thick layer of insulators. Depending on application purposes, the gate surface of the ISFET can be further modified by depositing other materials on the oxide layer such as Si_3N_4 for pH sensors [85-87], monolayer of polymer for biomolecular binding [42, 88], or *high-k* materials to enhance the electronic coupling with biology systems [82].

In the following treatment of the ISFET, it will be referred to the p-channel ISFET, which is composed of a *pnp*-structure, because most of the works in this thesis were based on p-channel transistor. However, all considerations apply in analogous manner to the n-channel ISFET.

Operation principle

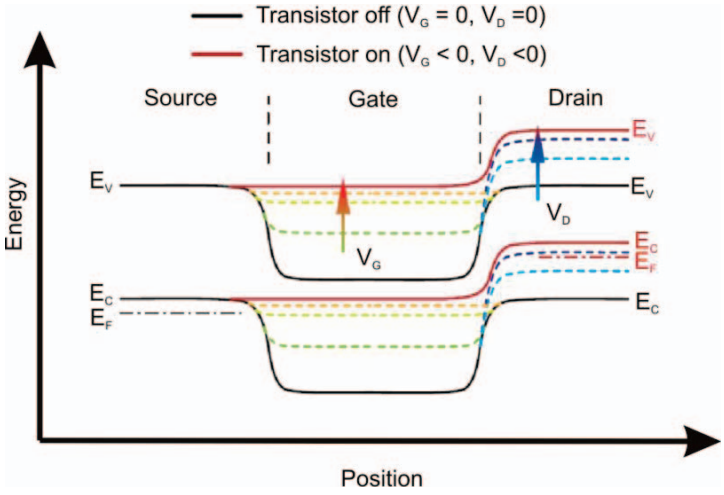

Figure 2.2. *Energy band diagram of a long channel p-channel transistor. The voltage applied to the gate reduces the energy barrier and thus forms a conductive channel between source and drain at the threshold voltage (V_{TH}). The black lines represent the transistor in an "off-state". The red lines represent the transistor in an "on-state". The dash colored lines show the relationship of the energy barriers on the voltage applied (Adapted from [89]).*

The operation of the ISFET is similar to the operation of a MOSFET device, where the gate voltage modulates the current between the source and drain, I_{DS}. This phenomenon can be physically explained by using a simple energy band diagram model of the device as shown in figure 2.2. In the equilibrium condition, due to the different free- charge polarity, the two *pn* junctions at source-channel and drain-channel interfaces form a built-in potential under flat band condition. The energy band bending caused by two *pn*-junctions forms a potential barrier under the gate. When the gate voltage equals zero (V_{GS} = 0 V), the charge carriers ("holes" in this case) cannot pass the channel due to potential barrier between the channel and the drain/source areas. Therefore, there is no current flow between source and drain even if a drain voltage is applied (V_{DS} < 0 V). When a gate voltage is applied (V_{GS} < 0 V), the potential barrier decreases with increasing gate voltage until it reaches the *threshold voltage* (V_{TH}). At this point, an inversion layer of charge carriers is formed under the gate area, thus, forming a conductive channel between source and drain. When a drain voltage is applied, an electric current flows between source and drain. With low drain voltages, the device operates like a resistor with the gate voltage

controlling the resistance, while under high drain voltage the device operates like a current source with the gate voltage controlling the magnitude of the current. More details about the FET devices can be found in several semiconductor text books [84, 90].

Characteristics

Potential drops across the ISFET with an applied gate voltage are shown in figure 2.3 [91]. They are the voltage drops at the reference electrode, the electrolyte solution, the oxide – electrolyte interface, the gate oxide layer and the silicon under the gate. They depend on the reference electrode type, the composition of the electrolyte solution, the gate oxide charges and the specific doping level of the silicon, respectively. Therefore, *threshold voltage* of an ISFET is defined as [92]

$$V_{TH} = E_{ref} - \Psi_s + \chi_{sol} - \frac{\Psi_{Si}}{q} - \frac{Q_{ox}+Q_{ss}}{C_{ox}} - \frac{Q_B}{C_{ox}} + 2\Phi_F \qquad 2.1$$

Φ_F is the potential difference between the actual Fermi level in the silicon between source and drain and the Fermi level of the intrinsic silicon. A potential change of $2\Phi_F$ at the silicon surface is generally defined as the onset of the inversion layer. E_{ref} is the reference electrode potential related to vacuum. The potential at the gate oxide-electrolyte interface is determined by the surface dipole potential of the solution χ_{sol}, which is a constant, and the surface potential Ψ_s, which results from a chemical reaction, usually governed by the dissociation of surface-oxide groups. Ψ_{Si} is the silicon work function, q is the elementary charge, C_{ox} is the capacitance of the gate oxide, Q_{ox}, Q_{ss} and Q_B are the fixed charges located at the oxide, the surface state density at the silicon surface and the depletion charge in the silicon, respectively.

For a real ISFET device, all contributions in equation 2.1 are in a first approximation constant except Ψ_s. The surface potential depends on the oxide-liquid interface, where the surface charge depends on the dissociation of the oxide surface group at different pH-values of the solution or by the adsorption of the charged molecules to the surface. Therefore, the ISFET is sensitive to the pH-value of the electrolyte and to the binding of biomolecules, realizing at the same time a pH sensor and a biosensor. It is important to note that the electrochemical reference electrode (RE) is necessary to keep the ISFET working reliably as it will be discussed later.

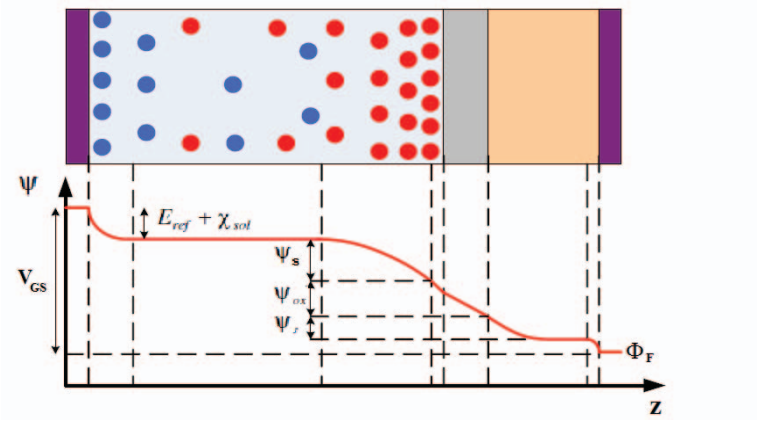

Figure 2.3. *Potential drops at gate electrode of an ISFET structure. The potential drop due to the reference electrode and electrolyte interface is (E_{ref} + χ_{sol}). The potential drop due to double layer at the electrolyte–insulator interface is (Ψ_s). The potential drop within the insulator is Ψ_{ox}. The potential drop due to the depletion charges in the semiconductor is Ψ_{si} (Adapted from [91]).*

If the gate voltage is higher than the threshold voltage ($V_{GS} > V_{TH}$), the source to channel barrier is large and the number of charge carriers in the channel is small. In this case, the diffusion of the charge carriers dominates and the drain current I_{DS} varies exponentially with (V_{GS}-V_{TH}) as given by

$$I_{DS} = \frac{W}{L}(m-1)\mu_{eff}C_{ox}(\frac{k_bT}{q})^2 e^{q(V_{GS}-V_{TH})/mk_bT} \qquad 2.2$$

where m= $1+\frac{C_D}{C_{ox}}$ with C_D is semiconductor depletion capacitance, μ_{eff}.is effective hole mobility. The subthreshold slope

$$S = 2.3m\frac{k_bT}{q} \text{ (mV/decade)} \qquad 2.3$$

shows the necessary increase in gate voltage to increase the drain current by a factor of 10. For a well-designed device, S is smaller than 80 mV/decade [90]. The theoretical lower limit is 60 mV/decade at room temperature.

When $V_{GS} < V_{TH}$, an inversion layer of hole carriers is formed under the oxide layer of the channel, thus, creating a conducting channel between source and drain. The holes density (Q_p) of the inversion layer per unit area parallel to the surface over the entire channel length L is given by

$$Q_p = WC_{ox}(V_{GS} - V_{TH}) \qquad 2.4$$

In this equation, W is the width of a transistor, C_{ox} is the gate oxide capacitance per unit area and V_{GS} and V_{TH} are the gate source voltage and threshold voltage, respectively.

An applied drain-source voltage causes Q_p to vary along the channel length, because the voltage drop across the gate oxide is now a function of the channel length. Assuming that the voltage drop at position *x* along the channel length is V(x), the hole density at position *x* is given by

$$Q_p(x) = WC_{ox}[V_{GS} - V(x) - V_{TH}] \quad 2.5$$

while the current at position x is equal to

$$I_D = WC_{ox}[V_{GS} - V(x) - V_{TH}]\mu_p dV(x)/dx \quad 2.6$$

Since I_{DS} must remain constant along the channel, V(x) and $dV(x)/dx$ must vary such that the product of V_{GS}-$V(x)$-V_{TH} and $dV(x)/dx$ is independent of *x*. The resulting relation between the drain current as a function of drain-source voltage V_{DS} and gate-source voltage V_{GS} is given by

$$I_{DS} = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}[2(V_{GS} - V_{TH})V_{DS} - V_{DS}^2] \quad 2.7$$

The nonlinear relationship between I_{DS} and V_{DS} reveals that the transistor cannot generally be modeled as a simple resistor. However, for a small drain voltage $|V_{DS}| << 2\ (|V_{GS}-V_{TH}|)$, equation 2.7 reduces to:

$$I_{DS} = \mu_p C_{ox}\frac{W}{L}(V_{GS} - V_{TH})V_{DS} \quad 2.8$$

This equation exhibits a linear relation between I_{DS} and V_{DS} for a given V_{GS} and the transistor behaves simply like a resistor.

If the drain voltage increases, the drain current reaches a saturation and becomes constant for $|V_{DS}| > |V_{GS} - V_{TH}|$. At the point where $V_{DS} = V_{GS} - V_{TH}$, the channel experiences a pinch-off state. Thus, further increase in V_{DS} simply shifts the pinch-off point toward the drain. In the saturation mode, the relation between the drain current and the voltage is given by

$$I_{DS} = \mu_p C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2 \quad 2.9$$

This equation applies for a long channel transistor, while the equation must be modified considering the channel modulation effect for short channel transistor [84].

The transconductance of an ISFET is the derivative of the drain current in dependence of the change of the gate voltage and can be determined from the transfer characteristic of the device:

$$g_m = \left.\frac{\partial I_{DS}(V_{GS})}{\partial V_{GS}}\right|_{V_{DS}=const} \quad 2.10$$

$$g_m = \begin{cases} \mu_p C_{ox} \frac{W}{L} V_{DS} & linear\ mode \\ \mu_p C_{ox} \frac{W}{L} (V_{GS} - V_{TH}) & saturation\ mode \end{cases}. \qquad 2.11$$

The maximum of this value is a measure for the quality of the device. A higher value corresponds to a larger change in the drain current for a given change in V_{GS}. For an ISFET device, this parameter is the most important one, because it reflects the sensitivity of the device.

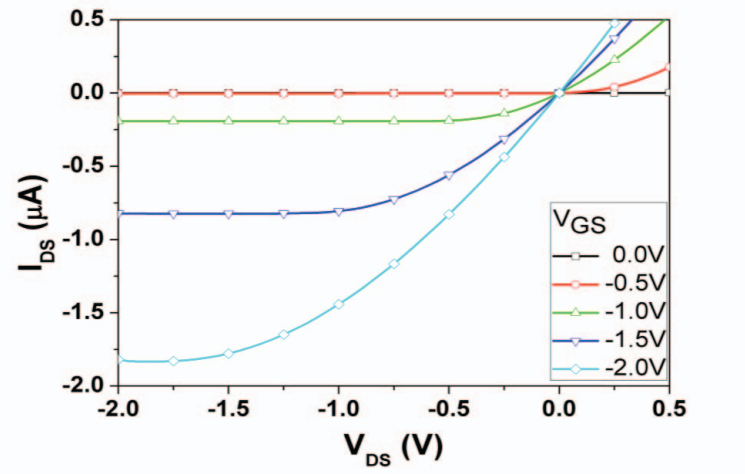

Figure 2.4. *Output characteristics of a p-channel ISFET device show the dependent of current on V_{DS} at constant V_{GS} values. At low V_{DS} the transistor behaves like a resistor while at high V_{DS} the current I_{DS} is saturating.*

Since the ISFET has three terminals, there are two ways to plot the characteristics of the transistor, namely the transfer and the output characteristics. The output characteristics displays the dependence of the drain source current (I_{DS}) to the drain-source voltage (V_{DS}) at constant gate-source voltages (V_{GS}), while the transfer characteristics displays the I_{DS} versus V_{GS} at constant V_{DS}. In figure 2.4 shows typical output characteristics of a p-channel ISFET measured in electrolyte solution of pH 7. The black and red curves (at V_{GS} = 0.0 V, 0.5 V) present the output current measured at V_{GS} below V_{TH}, I_{DS} is 0. The green, blue and cyan curves present the output current at V_{GS} above V_{TH}. At low $V_{DS,}$ the current is linearly dependent on V_{DS}, while at high V_{DS} the current is saturated and only depends on V_{GS}.

Figure 2.5 shows the transfer characteristics of the p-channel ISFET in linear and in logarithmic scales. On a linear scale, essentially no current flows until the gate voltage reaches the *threshold voltage*, V_{TH}. On the logarithmic scale, however, the drain current

increases exponentially for $|V_{GS} < V_{TH}|$. Above threshold voltage, I_{DS} varies as the gate overdrive, V_{GS} - V_{TH} to a characteristic power. Normally, the working point of an ISFET device is chosen at the maximum value of transconductance at a certain V_{DS}.

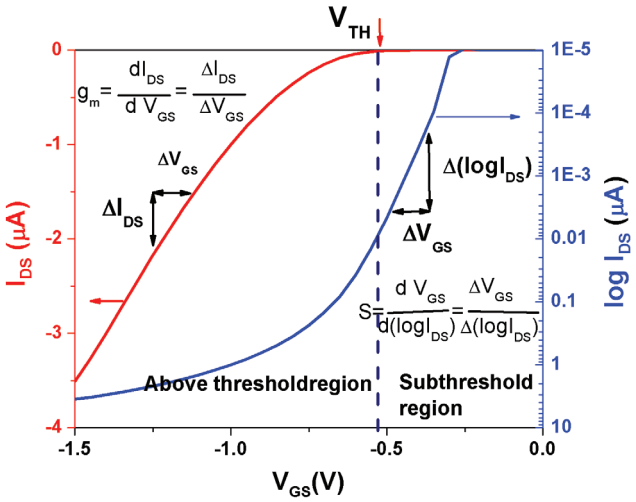

Figure 2.5. *Transfer characteristics of a p-channel ISFET showing I_{DS} (on a logarithmic scale on the left and a linear scale on the right) versus the gate–source voltage, V_{GS}. The transistor is considered to be switched on when V_{GS} is equal to the maximum voltage supplied to the device. The higher the slope in the subthreshold region ($V_{GS} < V_{Th}$), the better the transistor switch-on characteristics become. Above threshold, the change in I_D for a given change in V_{GS} is called the transconductance, g_m. The working point of an ISFET for a constant voltage mode is usually chosen at the maximum value of the transconductance.*

2.1.2. The oxide-liquid interfaces

When a silicon oxide surface is in contact with an electrolyte solution, surface hydroxyl groups (SiOH) are built up at the oxide-electrolyte interface. These hydroxyl groups are charged depending on the pH-value of the solution. The pH – value at which the surface is neutral, is called the point of zero charge (pH_{pzc}) (pH_{pzc} = 2.2 for SiO_2) [94]. At a pH lower than the pH_{pzc}, the oxide surface is positively charged and at a pH higher than the pH_{pzc} the surface is negatively charged. Consequently, at physiological pH value (pH ≈ 7), the net surface charge of silicon oxide is negative. In this section, the relationships between the surface potential Ψ_S and the pH-value of the solution, the surface charge density σ and the concentration of ions in the electrolyte are discussed.

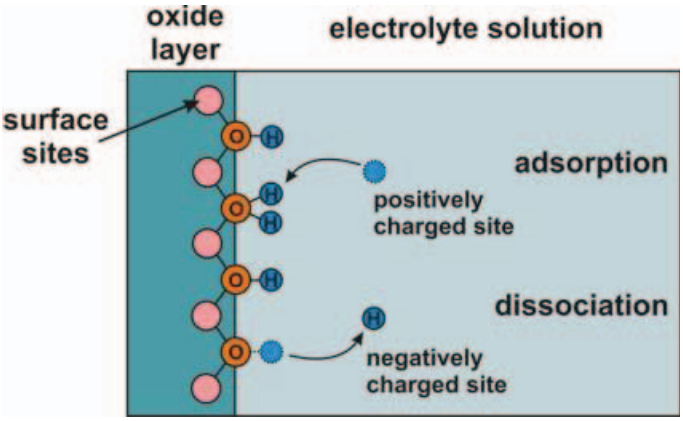

Figure 2.6. *Schematic illustrates the acid-base equilibrium (chemical reactions) on silicon oxide surface. The reaction involves the protonation and deprotonation of hydroxyl groups (OH) from the oxide surface. To which extent the one reaction exceeds the other is strongly influenced by the pH-value and determines the net surface charge [93].*

A general model of the surface potential Ψ_S changes per unit bulk electrolyte pH-value was developed by Bergveld's group [95]. Depending on the pH of the solution, the hydroxyl group at the oxide surface can protonate or deprotonate to form positive or negative charge as shown in figure 2.6 and build up an effective charge at the oxide surface. Due to this charge an electrostatic potential Ψ_s is developed in the electrolyte solution side near the oxide surface. This potential between electrolyte solution and oxide surface causes a difference of proton concentration between electrolyte bulk and surface that is according to a Boltzmann statistics:

$$a_{H_S^+} = a_{H_B^+}\, exp\frac{-q\Psi_s}{k_b T} \qquad 2.12$$

where $a_{H_i^+}$ is the respective activity of H^+ (proton), the subscripts S and B refer to the surface and the bulk solution, respectively; q is the elementary charge, k_b is the Boltzmann constant and T is the absolute temperature. Transformation of equation 2.12 yields the Nernst equation, which describes the relation at equilibrium between Ψ_s and the corresponding differences in the pH-value between bulk and surface:

$$\Psi_s = 2.3\frac{k_b T}{q}(pH_S - pH_B) \qquad 2.13$$

The capability of the surface to store charge as a result of a small change in the H^+ concentration at the surface is directly related to the intrinsic buffer capacity β_{int}

$$\beta_{int} = -\frac{1}{q}\frac{d\sigma_0}{dpH_S} \qquad 2.14$$

Because of charge neutrality, an equal but opposite charge with respect to σ_0 is build up in the electrolyte solution side at the interface. The two opposite charges form the so-called double layer capacitance C_{DL}. This value depends on the electrolyte solution and describes the amount of charge delivered from the bulk electrolyte to the interface upon a change in the surface potential:

$$C_{DL} = \frac{d\sigma_0}{d\Psi_s} \qquad 2.15$$

Combination of (2.14) and (2.15) leads to an expression for the sensitivity of the electrostatic potential Ψ_S towards the change of the pH-value at the oxide surface:

$$\frac{d\Psi_S}{dpH_S} = -q\frac{\beta_{int}}{C_{DL}} \qquad 2.16$$

Combining the Nernst equation and equation 2.16 gives a general expression for the sensitivity of the electrostatic potential to changes in the bulk pH-value:

$$\frac{d\Psi_s}{dpH_B} = -2.3\alpha\frac{k_bT}{q} \qquad 2.17$$

with

$$\alpha = (\frac{2.3k_bTC_{DL}}{q^2\beta_{int}} + 1)^{-1} \qquad 2.18$$

α is a dimensionless sensitivity parameter, and its value varies between 0 and 1 depending on the intrinsic buffer capacity and the double layer capacitance. The magnitude of β_{int} and C_{DL} relative to each other determine the deviation of the pH sensitivity from an ideal Nernstian behavior, which corresponds to a change of 59 mV/pH at room temperature (T = 300 K). However, in reality this maximum will not be reached as the surface SiO groups act as pH buffers. The following paragraph will discuss how β_{int} and C_{DL} are related to the structure and composition of the specific gate oxide and employed electrolyte solution, respectively.

Yates et al [96] developed a site-binding model to describe the charging mechanism of the oxide surface. According to this model, the charging of the oxide surface is the result of a thermodynamic equilibrium reaction between the surface hydroxyl groups (SiOH) and the H^+ ions of the bulk electrolyte solution. The reactions are:

$$SiOH \leftrightarrow SiO^- + H^+ \qquad K_a = \frac{[SiO^-][H^+]}{[SiOH]} \qquad 2.19$$

$$SiOH_2^+ \leftrightarrow SiOH + H^+. \qquad K_a = \frac{[SiOH][H^+]}{[SiOH_2^+]} \qquad 2.20$$

This chemical reaction shows that an originally neutral surface hydroxyl group can bind a proton from the bulk solution to become a positive surface charge with the dissociation

constant K_a, as well as to donate a proton to the solution, leaving a negative charge on the oxide surface with the dissociation constant K_b. It is noted that the K values at thermal equilibrium are intrinsically dimensionless and constant independent of the ionization state of the oxide surface. The relation between the surface activity and the bulk activity of H^+ is given by the Boltzmann equation. Depending on the chemical equilibrium of the surface sites, a surface charge density σ_0 exists:

$$\sigma_0 = qN_S \left[\frac{a_{H_S^+}^2 - K_a K_b}{K_a K_b + K_b a_{H_S^+} + a_{H_S^+}^2} \right] \quad 2.21$$

where N_s is the density of the available sites on the oxide surface. The pH dependent intrinsic buffer capacity of an oxide is

$$\beta_{int} = N_S \left[\frac{K_b a_{H_S^+}^2 + 4K_a K_b a_{H_S^+} - K_a K_b^2}{(K_a K_b + K_b a_{H_S^+} + a_{H_S^+}^2)^2} \right] 2.3 a_{H_S^+} \quad 2.22$$

This expression is valid for all oxides whose charging mechanism can be described by the association and dissociation of one *amphoretic* group. The values of N_S, K_a, K_b are oxide dependent.

Hiemstra et al. introduced a multisite complexation model (MUSIC) to describe the charging mechanism of oxides [97]. This model is based on crystallographic considerations and can be unified with the site-binding model. In this model, the charging of silicon oxide surfaces is completely dominated by the dissociation of individually coordinated, neutral groups so that the protonation of the silanol groups is negligible in the normal pH-value range. The intrinsic buffer capacity of the SiO_2 surface is given by:

$$\beta_{int} = N_S \left[\frac{K_a}{(K_a + a_{H_S^+})^2} \right] 2.3 a_{H_S^+} \quad 2.23$$

The oxide–electrolyte interface formed an electric double layer. The thickness of the double layer is usually given as being approximately 1.5 λ_D, where λ_D is the Debye–Hückel length:

$$\lambda_D = \sqrt{\frac{\epsilon_r \epsilon_0 k_b T}{2 n_0 z^2 q^2}} \quad 2.24$$

where n_0 is the bulk concentration of the electrolyte, ε_r is the relative dielectric permittivity of the solvent, ε_0 is the permittivity of the vacuum, k_b is the Boltzmann constant, T is the temperature, z is the ion charge, and e is the elementary charge. For $z = 1$, the approximate λ_D values calculated for electrolyte concentrations of 1×10^{-3}, 1×10^{-5}, and 1×10^{-7} M are 10 nm, 100 nm, and 1 μm, respectively. It is important to note that potential drops within the double layer and remain constant in the bulk electrolyte.

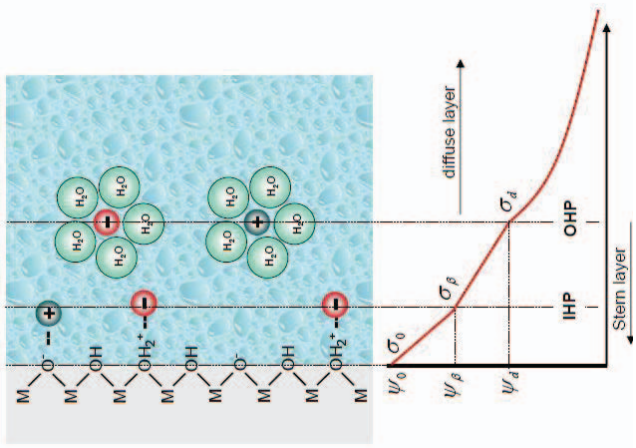

Figure 2.7. *Gouy – Chapmann- Stern model of the electric double layer build up at the interface between the oxide and the liquid with the potential drops over this layer (Adapted from [91]).*

There are several models to describe the double layer capacitance. The most widely used one is the Gouy-Chapman-Stern model, which describes the compensation of a surface charge by two consecutive layers of counter ions as depicted in figure 2.7. In the inner part, so called Stern layer, the ions are directly adsorbed to the surface and immobile. By contrast, in the outer part a diffuse layer exists composed of mobile ions, which obey Poisson – Boltzmann statistics [98].

In the Gouy – Chapmann model [99, 100], the excess charge at the solution side of the interface has an opposite sign and is equal in value to that of the solid state surface. The ions in the solution are therefore electrostatically attracted to the solid state surface, but the attraction is counteracted by the random thermal motion that acts to equalize the concentration throughout the solution. The equilibrium between these opposite trends is given by the well-known Boltzmann equation. The relation between the surface charge density and the surface potential is expressed as

$$\sigma_{DL} = -\sqrt{8k_bT\varepsilon_r\varepsilon_0 n_0}\,sinh\left(\frac{zq\Psi_s}{2k_bT}\right) \qquad 2.25$$

where ε_r is the dielectric constant of the bulk electrolyte, n_0 is the concentration of each ion in the bulk solution and z is the valance of the ions. This equation is called the Grahame equation. A differentiation of this equation with respect to Ψ_S gives the differential capacitance of the diffusion layer:

$$C_{DL} = \left(\frac{2z^2q^2\varepsilon_r\varepsilon_0 n_0}{k_bT}\right)^{1/2} cosh\left(\frac{zq\Psi_s}{2k_bT}\right) \qquad 2.26$$

The Gouy-Chapmann theory has one major drawback. All ions are considered as point charges that can approach the surface arbitrarily close. This assumption causes unrealistic high concentrations of ions near the surface at high values of ψ_0. Stern [98] introduced that ions cannot approach the electrode surface closer than their ionic radius. The distance of the closest approach is called the outer Helmholtz plane (OHP) or Stern layer.

The capacitance per unit areas of the Stern layer C_{St} can be estimated by the plate capacitor formula: introducing the half of the hydrated ion radius r_{ion} as the relevant distance between the charge sheets yields

$$C_{St} = \frac{2\varepsilon_0\varepsilon_r}{r_{ion}} \qquad 2.27$$

where ε_0 and ε_r are the permittivity of vacuum and the dielectric constant of the Stern layer, respectively. The total capacitance at the interface is a serial circuit of the Stern capacitance and a diffusion capacitance. It is given by

$$C_{DL} = \frac{r_{ion}}{2\varepsilon_0\varepsilon_r} + \left\{\left(\frac{2z^2q^2\varepsilon_r\varepsilon_0 n_0}{k_bT}\right)^{1/2} cosh\left(\frac{zq\Psi_0}{2k_bT}\right)\right\}^{-1} \qquad 2.28$$

2.1.3. ISFET responses to biomolecular binding

As mention above, the ISFET can be used for label-free electronic analysis of biomolecules by monitoring the electronic signal caused by variations in the charge density at the gate oxide-electrolyte interface. Currently, various kinds of biorecognition materials for biological analysis such as DNA, proteins, enzymes, and living cells have been applied to ISFET measurements. This application owes to their unique electrical and biological properties, thereby elevating the sensitivity and specificity of detection [101]. The ISFET type for distinct bioanalysis depends on the contained layer of immobilized biomolecules on the gate surface as bio- recognition probes. These probes include enzymes, antibodies, and DNA strands assorted concepts of biosensors like enzyme FETs, immune FETs, and DNA FETs [102]. The detection principles of biomolecules are usually based on two mechanisms: i) a change of the surface potential at the oxide-electrolyte interface. ii) a change of input impedance of the ISFET, due to the binding of charged molecules at the interface or local changes in the electrolyte composition. Details about these mechanisms are given in the following subsections.

Charge-based detection

Biomolecules such as DNA or proteins adsorbed onto the oxide change the surface charge density at the oxide-electrolyte interface, which result in a change of the surface potential

according to the Grahame equation (equation 2.25). For DNA detection, for example, single-stranded DNA (called probe DNA) is immobilized on the gate surface. The probe molecules bind with a complementary single-stranded DNA presented in the electrolyte to form a double-stranded DNA, the DNA hybridization process (detail in section 3.9). An extra charge generated from the hybridization process of the target DNA from the surrounding solution to the probe DNA on the gate changes the threshold voltage of the transistor. The signals from different sensor approaches achieved by DNA hybridization were reviewed by Poghossian et al. [103]. The change of the surface potential due to the DNA corresponds to the change of the threshold voltage of different ISFET devices had a large variation in related literatures from several to hundreds of mV. An example of real time charge-based detection of DNA hybridization using a micro-scaled ISFET is shown in figure 2.8 [46]. The changes of the surface potential after immobilization of the 20 base pair probe DNA on the gate surface and after DNA hybridization were 4 mV and 6 mV, respectively. The immobilization process takes place within a few minutes, while the hybridization process takes much longer (about 60 minutes).

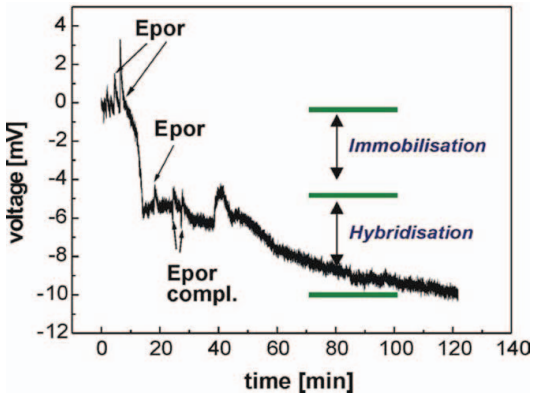

Figure 2.8. *Real time, label free detection of immobilization and hybridization of DNA by an ISFET. The change of the sensor signal relates to the adsorption of DNA molecules on the gate surface. (Epor receptor: 5-ACTCATTCTCTGGGCTTGG-3) [46].*

As discussed in subsection 2.1.2, the surface potential depends on the dissociation of the hydroxyl group in thermal equilibrium in response to changes of the pH-value. However, it also responds to other changes of the electrolyte composition. If the hybridization process changes the amount of charge in the DNA layer, the hydroxyl groups response by absorbing or releasing hydrogen ions, or by changing the local concentration of the electrolyte. The level of complexity of those effects including the adsorption of charged

biomolecules and the change of the local pH-value or ion concentrations leads to difficulties in predicting the change of the surface potential, and maybe affects the device sensitivity. The mechanisms underlying the charge-based detection are still under discussion, however, there are several models used to explain the change of the surface potential based on these effects.

According to Poghossian et al. [103], probe ssDNA-molecules arranged with a center-to-center average interprobe distances are immobilized to a part of the surface of an ISFET, while the remaining surface between the immobilized molecules stays in contact with the electrolyte solution. For probe ssDNA, depending on the immobilization process, the DNA molecules can align perpendicular or in a certain angle to the surface. Caused by the hybridization, the target molecules binding to the probe realize a redistribution of the ion concentration in the intermolecular spaces or the alteration of the ion sensitivity of the transducer. These resulting changes in the potential at the intermolecular regions can be detected by the ion sensitive field-effect sensor. Assuming a high density of the immobilized ssDNA of about $2x10^{13}$ molecules/cm^2 and 100% hybridization efficiency in the high electrolyte concentration of 0.5 M, the change of the sensor signal as predicted by this model is about 28-35 mV. This effect depends on the ionic strength of the bulk electrolyte solution, and is stronger in a solution with low ionic strength.

Landheer at al. [104, 105, 106] proposed a model based on the potential drops across the EIS structure for the sensitivity of FET-sensors used to detect charged macromolecules in the electrolyte solution. This model considers structures where the oxide has *amphoteric* surface sites that have been functionalized. In this model, the layer of biological charged macromolecules is considered as a planar ion-permeable membrane, whose potential profile is described by the Poisson–Boltzmann equation. Target biomolecules such as proteins or single-stranded DNA fragments dissolved in electrolytes are considered as charged molecules surrounded by a diffusion layer of counter-charge. A hypothetical DNA hybridization experiment explainable by this model suggests the use of low concentration electrolyte solutions to obtain considerable change in the surface potential for uncharged insulator surfaces with and without oligonucleotides on the surface. Both of these models, however, can only explain the small signal experiment as summarized in reference [103]. A model for the larger changes of the signal described in other publications is still not existing.

Recently, Wunderlich et al. [107] discussed the importance of three sensitivities of the gate interface - the sensitivity to the density of biomolecular charges, the sensitivity to changes

in ion concentration, and the sensitivity to changes in the pH-value. In this model, the biomolecules to be detected bind with high affinities to specific receptors on the surface, and thus irreversible binding of the charges can be assumed. The receptors are assumed to be located in the same plane as the acid-based charges originating from the protonation and deprotonation of titratable surface groups, e.g. *amphoteric* OH groups on the SiO_2 gate of the ISFETs. The authors concluded that a quantitative detection of charged molecules by FETs is optimally achieved on surfaces with both low pH-sensitivity and low surface potential, which corresponds to a low response to pH-value and electrolyte concentration changes. Further improvements to this model were introduced by McKinnon et al. and can be found in a recent publication [108].

Impedance-based detection

The binding of biomolecules to the gate surface can also be detected via an impedimetric method as described below. The binding to the gate surface changes the input impedance of the interface leading to a change of the total impedance. When applying an AC signal to the gate input, the response of the ISFET to the applied signal depends on the frequency of the signal. The adsorption of biomolecules such as DNA hybridization or protein interaction on the surface causes a change of the frequency response of the ISFET [35, 42-45, 109, 110].

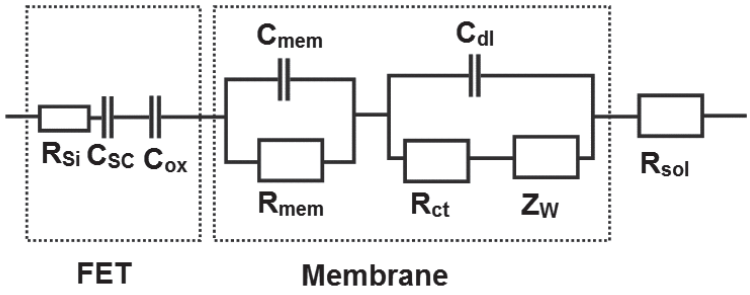

Figure 2.9 *Equivalent circuit of an ISFET including the contribution of the FET, the oxide-electrolyte interface, and the bulk solution. The biomolecule-membrane at the oxide-electrolyte interface is described by capacitor (C_{mem}) in parallel with a resistor (R_{mem}) [35].*

An ISFET with a membrane of biomolecules on top of the gate is generally expressed as an equivalent electronic circuit as shown in figure 2.9. The underlying ISFET contributes to the total impedance by the silicon-electrode resistance (R_{Si}) in series with a space-charge capacitance (C_{SC}), and the capacitance of the oxide layer (C_{ox}). When the ISFET is

operated in inversion, the space-charge capacitance can be neglected in comparison to the oxide-layer capacitance. The membrane bulk impedance is described by a bulk resistance (R_{mem}) in parallel with a bulk capacitance (C_{mem}). The interfacial part of the membrane impedance consists of the double-layer capacitance (C_{DL}), the resistance of the charge transfer at the interface (R_{CT}), and a contribution from the diffusion of ions, described by the Warburg impedance (Z_W). If interfacial effects to the membrane impedance are detectable, this generally occurs at low frequencies (<5 Hz). However, the rapid exchange of ions at the interface results in a charge-transfer resistance that is too small to observe [35, 44].

The last components included in the equivalent circuit are the contributions of the electrode and the electrolyte solution, R_{sol}. Experiments showed that the impedance response of ISFETs is strongly depending on the ion concentration of electrolyte solutions as well as the distance from the reference electrode to the gate surface. This effect can also utilize for determination of conductivity of an electrolyte solution [111].

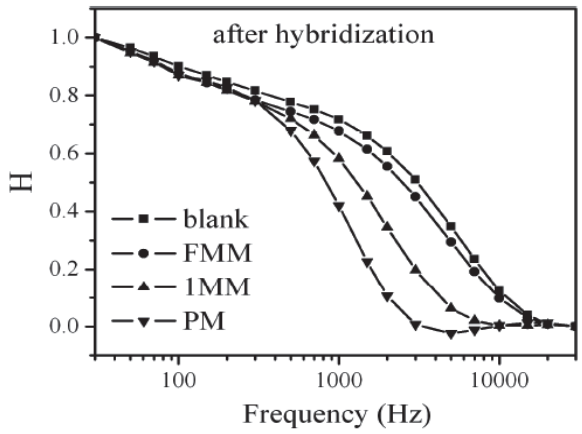

Figure 2.10. *Frequency response of an ISFET after DNA hybridization of different mismatches of target DNA binding to the probe ssDNA, which was previously immobilized on the gate surface of 4 transistors of the 16-channel device [43].*

The equivalent circuit for the gate input can be described by a transfer function. The transfer function is the mathematical representation of the relation between the input and the output signals of a frequency-dependent system. Biomolecular interactions at the gate oxide make a change in the membrane impedance and lead to a change in the frequency-dependent of the transfer function.

$$H(j\omega) = \frac{1+j\omega R_{mem}C_{mem}}{1+j\omega R_{mem}(C_{mem}+C_{ox})} \quad 2.29$$

Figure 2.10 shows an example of DNA hybridization detection via an ISFET's transfer function [43]. By employing this technique, the authors were able to detect a single nucleotide mismatch of the target DNA sequence.

2.2. Silicon nanowire (SiNW) FET biosensors

The current revolution in applied life sciences is strongly linked to the availability of new experimental tools that enable the manipulation of biomolecules and the study of biological processes at the molecular level using state-of-the-art nanomaterials and nanotechnology [128]. The progressive downscaling of the technology has created materials with at least one critical dimension in the range from few nanometers up to several hundreds of nanometers. There are two main reasons for the exploration of matters in the nanometer range: Firstly, the nanoscaled materials are comparable in size with most biological objects such as proteins, DNA, cells or viruses etc., making them as an ideal interface between biological systems and sensor devices. Secondly, the nanoscaled materials possess new physical and chemical properties arising from their size. A high surface-area-to-volume ratio of the nanoscaled materials causes the surface atoms to play an important role in determining the physical, chemical and electronic properties of the devices. The surrounding interface change the properties of the nanomaterials make them excellent substrates for biomolecular sensing.

Recently, a diversity of nanoscaled sensor types such as cantilevers [30, 112], carbon nanotubes [113-117], quantum dots [23, 63, 118-120], semiconductor nanowires [121-124], and nanogaps and nanopores [125, 126] have been designed and fabricated that utilize different nanomaterials as a transducer to sense biomolecules. However, advantages of sensors designated to operate like ISFETs over the other transducers are that nanoFETs can directly translate the biological interaction into a recordable electric signal. Sensors based on nanoFETs promise to revolutionize bioanalytical research by offering a direct, real time, highly specific, ultra-sensitive method for label-free detection of biomolecules [61, 127, 128]. In this category, the silicon-nanowire field-effect transistor (SiNW-FET) is widely studied for biochemical sensing, since it utilizes the well-understood silicon technology in contrast to other FET-types like carbon nanotubes or oxide semiconductor nanowires.

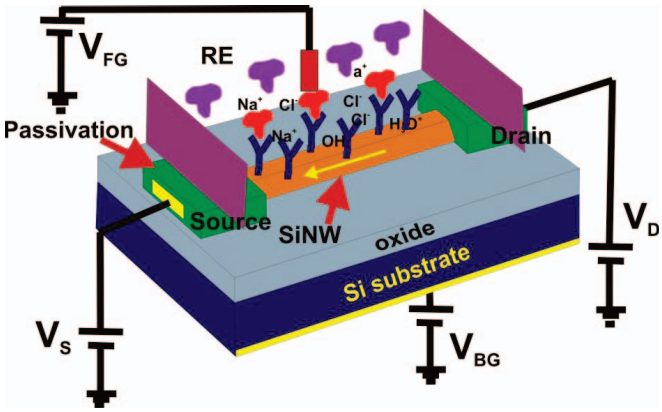

***Figure 2.11**. Structure of a SiNW-FET device used as a biosensor. As an ISFET, the device consists of source and drain contacts at the terminal of the nanowire. The wire and the source-drain contacts are separated from the Si substrate by a SiO_2 layer providing the SiNW-FET with the possibility to be operated using either the back-gate or front-gate contact. In most reported cases, the back gate was employed due to the limitation of the front gate, which always needs a reference electrode and prohibits the device from being miniaturized.*

A structure and an electric configuration of a SiNW-FET sensor are depicted in figure 2.11. The SiNW-FET consists of four terminals: the source and drain electrodes, which have direct contact to the SiNW, the back gate (BG) electrode which is connected to the Si substrate, and the front gate (FG) electrode is the reference electrode and electrolyte solution. The back gate and front gate can separately control the SiNW operation or couple together to control the devices operation. It means that I_{DS} can be modulated by either the back-gate voltage (V_{BG}), or the front-gate voltage (V_{FG}), or both at the same time. This mechanism is explained in detail in the publication of Elibol et al. [129]. The electronic characteristics of a SiNW-FET are in principal similar to the characteristics of ISFET devices, which were described in detail in section 2.1.1. However, the different dimensions of the devices have to be considered, since the width of the SiNW-FET is very small compared to the width of the planar ISFET. This relation is given by [130]:

$$I_{DS} = \mu_p \frac{C_{ox}}{L^2}(V_{GS} - V_{TH})V_{DS} \quad \text{(linear region)} \qquad (2.30)$$

and

$$I_{DS} = \mu_p \frac{C_{ox}}{L^2}(V_{GS} - V_{TH})^2 \quad \text{(saturation region)}, \qquad (2.31)$$

where L is the length of the SiNW and C_{ox} is the gate oxide capacitance. The value of C_{ox} for a cylindrical can be calculated according to equation 2.32:

$$C_{ox} = \frac{2\pi\varepsilon\varepsilon_0 L}{\ln\left(\frac{2h+r}{r}\right)} \quad (2.32)$$

where h is the thickness of the gate oxide, and r is the radius of the silicon nanowire.

The working principle of a SiNW-FET device as a biosensor is similar to the ISFET sensor described in section 2.1.2 and 2.1.3. Therefore, the device is also sensitive to detect charged biomolecules that bind to the surface of the SiNW. However, this device shows a much higher sensitivity over the conventional micro-scaled ISFETs. One of the reasons is due to the high surface-to-volume ratio of the SiNW, the charge carriers inside the nanowire are highly influenced by the surface charges of the biomolecules binding at the SiNW's surface. Furthermore, due to the comparable size between the biological systems and the cross-section of the SiNW sensors (figure 2.11), the SiNW need less molecules to generate a visible signal compare to the planar ISFET. Nair et al. [22] used a simple scaling-relationship model based on diffusion limited transport of analyte molecules to compare the sensitivity and the response time of nanodevices and planar micro-scaled ISFETs. As shown in figure 2.12, the response time of biomolecules binding to the probe molecules on the surface of the SiNW is much faster than that on the normal planar ISFET. The figure also shows that the detection limit of typical nanowire sensors can be down to the femtomolar level of analyte concentration, while for planar ISFETs, the detection limit is in the picomolar range of the analyte concentration and the necessary time to achieve this detection is much higher (in the range of 10^9 seconds), which is more than 31 years.

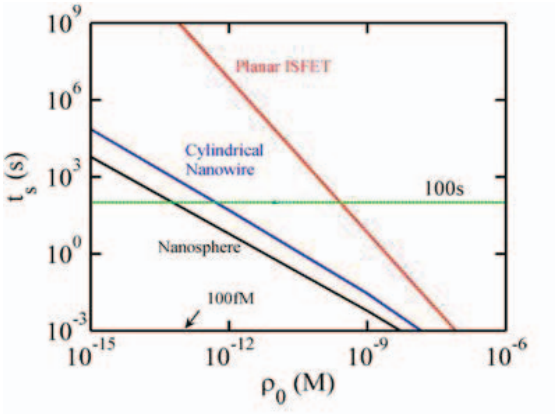

Figure 2.12 *Relationship between the response time (t_s) and detectable concentration of the analyte (ρ_0) for different sensor configurations. For a detection time of 100 s, the cylindrical nanowire system can detect picomolar concentrations, while a planar system can detect only in the nanomolar range (Adapted from [22])*

In the following, the use of SiNW-FETs for biosensing applications is reviewed. A decade ago, scientists of C. Lieber's group at Harvard University firstly utilized SiNW field-effect devices as biosensors and bioelectronics interfaces [127]. A "bottom-up" approach was used to fabricate boron-doped SiNWs by the nanocluster-mediated vapor-liquid-solid-growth method. The SiNWs were later aligned between two metal electrodes on a SiO_2/Si substrate to realize an electric contact [10, 127]. The SiNW-FET sensors were highly sensitive and enabled real time electrical detection of biological and chemical species. The amine- and oxide-functionalized SiNWs exhibited a pH-value-dependent conductance and were linear over a large range of pH-values (between 2 and 9). The above mentioned publications also show that the devices are capable to detect the streptavidin or m-antibiotin binding to biotin-functionalized SiNWs with a streptavidin concentration down to the picomolar range or a m-antibiotin concentration down to 10 nM. The devices show a linear change of the conductance at low concentrations of the analyte and are saturated at higher concentrations. Calmodulin-functionalized surfaces of the devices enable to reversibly detect Ca^{2+}-ion binding with a concentration of 25 μM. This could lead to the application of studying biological activity processes such as muscle contraction, protein secretion, cell development and death. Additionally, Lieber's group also showed that the SiNWs can be used as ultrasensitive sensors for the detection of DNA hybridization with concentrations of target cDNA down to 10 fM [55]. Further publications by the same group reported that SiNW-FETs are able to detect small molecules such as ATP [63], multiplexing cancer cells [65], and even single viruses [60] and studied neuronal signal [10]. The results of Lieber's group show that such devices are ultrasensitive as biochemical sensors and have an extremely broad range of applications in medicine and life sciences.

Following these pioneering work, there was an extremely increase of research on SiNW sensors for bioelectronic applications. To overcome the inherent problems of a "bottom-up" approach, "top-down" approach are mostly used to fabricate SiNW sensors nowadays. The details of nanowire fabrication are discussed in section 3.1. Z. Li et al. [70] introduced a silicon nanowire transistor, which was structured by electron-beam lithography (EBL) and etched by reactive ion etching (RIE) on silicon-on-insulator (SOI) wafers, with wire diameters ranging from 50 to 800 nm. These devices showed the possibility to detect the DNA hybridization process of target cDNA to ssDNA-functionalized nanowires. In this publication, it was shown that smaller nanowires are more sensitive than larger ones. However, the noise of the devices increases with decreasing size of the wire. In this experiment, the author demonstrated the sensitivity of the device to be 25 pM of target

DNA in pure water. The device's response was fast with a detection time of less than 50 s. The conductance of p-type NW was found to be 46% increased, while it was decreased by 12% for an n-type device.

Bunimovich et al. [52] used arrays of 400 SiNWs with a wire diameter of 20 nm for DNA detection, which were fabricated by the superlattice nanowire pattern transfer (SNAP) method [71]. Interestingly, the author demonstrated that the SiNWs can be used for real time DNA hybridization detection under electrophysiological conditions (1xSSC, concentration 0.16 M), which is generally accepted to be impossible with micro-scaled ISFETs. In this experiment, the probe-DNA was immobilized on the SiNWs using two different methods. In the first approach, the probe-DNA was electrostatically adsorbed onto a Poly-L-Lysine coated surface of the native oxide SiNW. In the second approach, the probe-DNA was selectively and covalently immobilized on the alkylated non-oxidized SiNWs. With the first method, the detection limit of the devices was 1nM of target DNA in 1xSSC buffer, while the second method resulted in a much higher sensitivity with a detection limit down to 1 pM of target DNA in the same buffer solution. In this publication, the authors claimed that there was no signal of the DNA hybridization in pure water, because of the significant ssDNA-ssDNA repulsion in pure water, while in the physiological solution the DNA hybridization is more efficient with a high ionic strength. The ability to detect DNA under physiological conditions may allow the use of SiNWs to detect biomolecules in direct biological samples such as serum or tissue culture media. Furthermore, this publication also shows the importance of controlling the surface chemistry of SiNWs for their optimization as biological sensors.

Stern et al. [61] demonstrated ultra-highly sensitive Si nanowire sensors that were fabricated by a different approach. In this case, the nanowire sensors were fabricated by e-beam lithography and RIE on a thin oxide layer on top of a SOI wafer. These structures were then transferred to the thin Si layer underneath by wet anisotropic etching using a TMAH solution. These devices showed a sensitivity, which was much better compared to the report by Z. Li [70] and in the same range as with nanowires fabricated by a bottom-up approach [55]. The detection limit of these sensors was reported as low as 10 fM for streptavidin binding to a biotin-functionalized nanowire. This improved sensitivity was caused by the wet Si etching process, which produced very smooth silicon surface and reduce the number of defects at the surface of the silicon nanowire to a minimum.

Recently, many other research groups continue to employ SiNWs as ultrasensitive biosensors [54, 131]. SiNW sensors can be regularly fabricated by "top-down" approach

using EBL, deep ultraviolet lithography (DUV lithography) [54, 68] or nanoimprint lithography [62, 75] or other lithography technologies to define the structures in combination with size-reduction strategies such as self-limiting oxidation or anisotropic etching of Si. Gao et al. [54] used a combination of DUV lithography with a self-limiting oxidation to produce SiNWs with widths even smaller than the resolution of an e-beam writer ranging from 5 to 50 nm. The devices showed a detection limit of 10 fM of target DNA.

The reported sensitivities of the different SiNWs for biomolecular detection shows vary from nM to fM or even aM of analyte concentration. Also the used buffer solutions are greatly varying from pure H_2O to physiological electrolytes. The detection mechanism of these SiNW biosensors is under discussion. However, the related theory that described above (section 2.1.3) can also be partly applied for the SiNW biosensors.

2.3. Nanofabrication techniques

Nanostructures can be fabricated by different techniques, which can be divided into two main categories: a “bottom up” approach and a “top down” approach. Typically a “top-down” approach is based on lithography techniques such as EBL or DUV lithography. In recent years, nanoimprint became popular as a low cost technique for nanofabrication with high throughput. Anisotropic etching of Si by TMAH is commonly used for micromachining. This also became available as a strategy for the size reduction for fabrication of nanoelectronic devices with high electrical performance. This section will discuss the principles as well as the feasibility of these techniques for SiNW sensor fabrication.

2.3.1. Nanoimprint lithography

Nanoimprint lithography (NIL) was proposed in 1995 when Stephen Y. Chou firstly reported sub-25 nm holes made in polymethylmethacrylate (PMMA) polymer with an imprinting mold [132]. This new technology was proposed to replace the expensive DUV lithography or EBL, with the same level of lateral resolution or better but at a fraction of the cost. It is a parallel process, just as optical lithography, but without the diffraction-induced limit on structure resolution like in optical lithography and in addition it does not suffer from the *proximity effect* like e-beam lithography. The nanoimprint process has been applied for high throughput fabrication of a wide range of nano devices such as electronic

[133-136], optical and photonic devices as well as for structuring of patterns for biological applications [137, 138]. In 2003, the International Technology Roadmap for Semiconductors (ITRS) included NIL as one of the next-generation lithography candidates for 32 nm technology and was kept as a candidate for the 22 nm technology on the 2009 released roadmap [139]. The mechanism and relevant parameters of this technique have been studied in detail in the last 15 years of development [140-149].

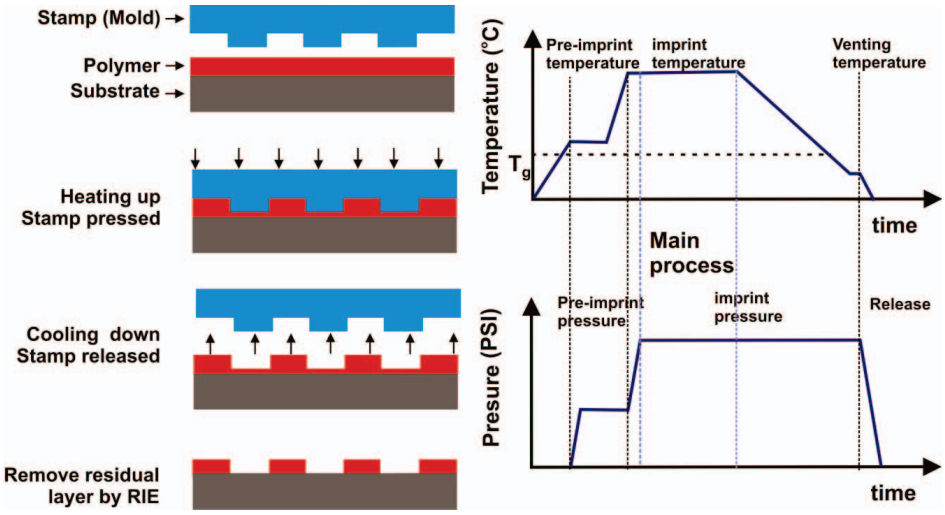

Figure 2.13. *Schematics show the principle of a thermal nanoimprint process (left), and related temperature and pressure profiles during the process (right).*

The principle of thermal NIL that was used in this thesis is illustrated in figure 2.13 and can be explained as following: A substrate with surface relief structures, as called *imprint mold* or *mold,* is aligned on a substrate, which has been coated by a thin layer of a thermoplastic polymer. The mold and the substrate are aligned and heated above the glass transition temperature of the polymer so that the polymer is softened and can flow. When the final temperature is reached the mold is pressed into the thin polymer layer at a pressure in the range of 30 to100 bars, depending on the viscosity of the molten polymer and the cavity of the relief structures. As the imprint depth is less than the polymer thickness, the mold surface does not have a direct hard contact with the substrate and such damage of the mold and the substrate is prevented. After that, the temperature is decreased below the glass transition temperature of the polymer and the pressure is released at a certain temperature called the *demolding temperature* or *venting temperature* and the mold is decoupled from the substrate. The temperature and the pressure profile at different stages of the imprint process used in this thesis are plotted on figure 2.13 (right). After the mold

separation, nevertheless, the polymer layer still covers the whole wafer just the thickness of the polymer differs within the structures. In a final step the residual layer of the polymer inside the imprinted pattern areas is removed by reactive ion etching (RIE). The polymer patterns obtained after removal of the residual layer is in the same as those obtained by optical lithography or EBL.

In this technique there are numbers of key factors needed such as the mold properties, the designed structure cavities, the polymer properties, the separation step and especially the RIE process to establish a reliable process and a high aspect ratio of the transferred structures.

The reliability of nanoimprint depends on the size and distribution of the sample structures; this is called the "*imprint-proximity effect"*. Nanoimprint relies on displacement of a polymer layer into the cavities of a structured mold. Depending on the applied pressure, time and the viscosity of the polymer, this can lead to systematic effects over the long distances. For example, dense arrays of structures will displace more polymers and depending on the distance of the structures, this may not imprint correctly due to the polymer displacement over long distances and subsequent thickening. In the same way, smaller features are easier to imprint than larger features, because bigger features generally need more polymer material and filling takes more time and may not fill up completely resulting in defects. However, the viscosity of the polymer decreases as the temperature increases so that the imprint of a big cavity is faster at high temperature. This *proximity effect* leads to defects of the structures and a different thickness of the residual resist layer in different parts of the sample, where the lateral structures are different.

The resolution of the nanoimprint process transfer to the polymer layer is mainly dependent on the resolution capability of the mold fabrication. Main requirement for the polymer are the low glass temperature to enable a low imprinting temperature, low viscosity to facilitate the flow of the polymer during the mold filling process, low shrinkage after imprinting to maintain the pattern fidelity and the polymer needs to have high resistance to the RIE process to serve as a mask for the structure transfer via RIE.

As discussed above, the most difficult task of the imprint lithography is imprinting both large and small structure at the same time. While the small feature can be imprinted quickly, large features may not get filled up completely. Another factor that affects the imprint results is the structure of the patterns. The residual layer after the imprint depends on the distribution of the cavities and the protrusion structures. The more uniform the distribution, the more uniform the residual layer is.

In the last step of removing the residual layer by RIE, which is carried out under oxygen plasma, is indiscriminative, it etches both, the residual layer and the imprinted polymer pattern structure. Depending on the relationship between the thicknesses of residual layer and the structures – the so called aspect ratio - the process has to be controlled precisely so that the thickness of structured polymer is large enough to guarantee a reliable process. If the polymer distribution was inhomogeneous and the variation of the residual layer was large, then this might result in pattern damage and distortion.

2.3.2. Anisotropic Si etch using TMAH

In order to avoid RIE of the active silicon layer, which degrades the device performance [77-79], TMAH was chosen to etch the Si device layer as it is very selective to SiO_2 or metals and etches anisotropically [150, 151]. TMAH etches the Si (111) plane much slower than others [150-152]. Lui et al. [80] has shown excellent electronic properties of a nano-FET device fabricated by e-beam lithography and subsequent etching by TMAH on SOI (110) compared to the same device fabricated by RIE. Many recent SiNW fabrication processes for bioelectronic applications have employed TMAH etching as a powerful tool to fabricated robust and highly sensitive devices [61].

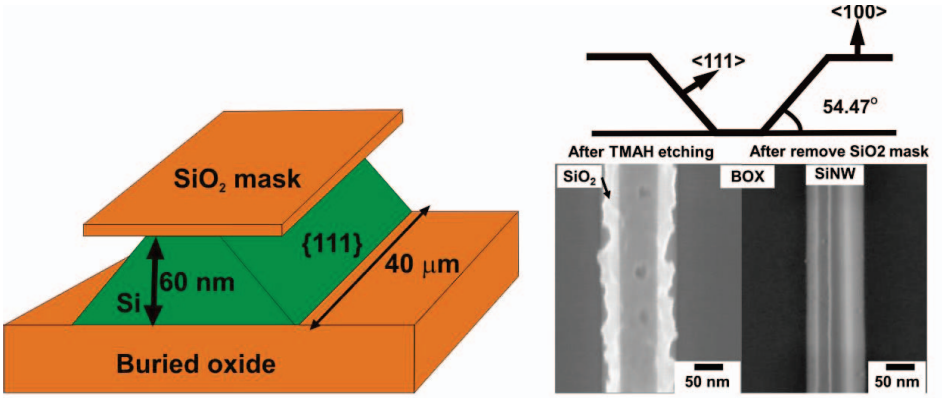

Figure 2.14. *Schematics of the anisotropic TMAH etching process of Si on a SOI wafer to create SiNWs. The bottom right picture shows an SEM image of SiNW produced by TMAH etching on SOI structure after 1 minute etching. The etching rate of other planes is much faster than the (111) plane, which created a SiNW longer than the defined structure.*

The principle of the TMAH etching process of Si on a SOI (100) wafer is shown in figure 2.14. A thin layer of oxide or nitrite on top of Si layer acts as a hard mask to protect the Si layer underneath. The TMAH solution is etching the exposed Si layer. The Si anisotropic

process creates a (111) plane sidewall which has an angle of 54.7^{o} to the (100) plane. The resulting Si nanowire has a trapezoidal cross-section under the oxide mask layer. With the high etching rates into the Si (100) plane in combination with the etch stop layer of the BOX, a short etching time is needed to etch down the device layer. Due to the anisotropic etching, all other planes are etched much faster than the (111) plane and all the defect roughnesses projected from the SiO_2 mask layer are eliminated. This is resulting in SiNWs with very smooth surfaces compared to the dry etching by RIE. Furthermore, the size of the nanowire under the mask can be tuned by different etching times.

Chapter 3. Materials and methods

The purpose of this chapter is to introduce properties of materials as well as experimental techniques that were used throughout this thesis. The first part of this chapter gives details of the "top-down" SiNW fabrication protocol used in this work. The methods for chip packaging, the setup for electric characterization and biomolecular detection of SiNW devices, and the chip cleaning and surface functionalization protocols for biomolecular binding are described in section 3.2, 3.3 and 3.4, respectively. Sections 3.5 to 3.9 introduce the methods for the distinguished biochemical sensing experiment such as pH sensitivity, the detection of Ca^{2+}, proteins and DNA molecules.

3.1. SiNW fabrications

In this thesis, a novel "top-down" approach for wafer-scale processes of SiNW arrays was developed based on a combination of nanoimprint lithography and wet anisotropic etching of Si on SOI wafer. Devices were fabricated at the clean room facility of the Institute of Bio- and Nanosystems (IBN), Research Center Juelich. For the complete sensor fabrication process, we employed nanoimprint lithography and anisotropic etching of Si by TMAH in combination with other micro-fabrication techniques such as wet etching, dry etching and photolithography to create the SiNW array sensors [62, 75]. Nanoimprint lithography, as discussed in subsection 2.3.1, is the high through put technique for nanostructures

fabrication. TMAH etching of silicon (details in subsection 2.3.2) is a simple technique with mass production capability.

The following paragraphs will discuss our chip design for biosensor applications as well as the different process steps. The critical points of each fabrication step are pointed out and the improvements of the individual steps from the first to the second generation of chip design and fabrication are highlighted and discussed [62, 75].

3.1.1. Sensor designs

In this work, two different generations with two different layouts of the SiNW arrays were fabricated.

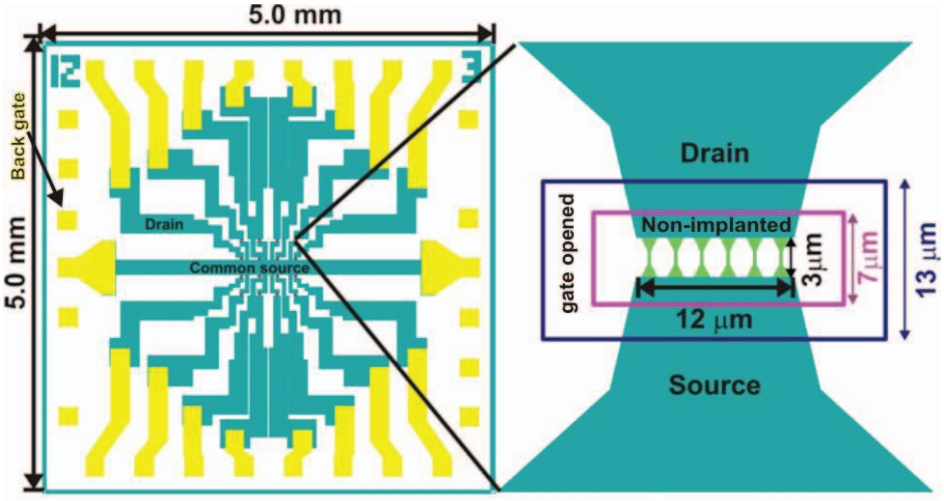

***Figure 3.1**. Layout of the 4×4 SiNW sensor array with common source contact (left) and the gate area of the array (right). In this first design, one gate consists of six nanowires in parallel having a length of 3 µm. The open gate areas is 13 µm × 24 µm and the non-implanted areas are 7 µm × 20 µm between source and drain contact line, respectively.*

In the first sensor design, the SiNW chips were mainly based on 4 × 4 arrays of SiNW sensors, which was compatible with the classical ISFET design of our group [9, 153, 154]. Only at the gate areas, the design was modified for the SiNWs taking the special chip processing protocol into account. In this design, some test chips of high density arrays of SiNWs (16 × 16 and 32 × 32 arrays) were added, that will in future be used for highly multiplexed detection and for the electronic coupling experiments with living cells [66, 72]. The chip size was 5 × 5 mm enabling a parallel processing of 130 chips on a single 4" wafer. The layout of the standard 4 × 4 sensor array having a pitch of 200 µm between

each nanowire area is shown in figure 3.1 (left). The chip included quite long contact lines for 16 individual drains and a common source contact to the nanowires. The contact lines and nanowires (blue areas) were fabricated by nanoimprint lithography, while the metal contacts (yellow areas) were fabricated by a lift-off process at the end of the chip fabrication protocol.

Each sensor of the array consisted of six nanowires in parallel. The length of the nanowires was fixed to 3 µm in all designs. The widths of the wires were varied from chip to chip by 100 nm, 200 nm, 500 nm and 1 µm (mask measures), respectively, to investigate the effect of the nanostructure size to the electronic performance. The source and drain contact lines were highly implanted with boron ions, while doping level of the nanowires was not changed in comparation to the original SOI wafer doping level. The transition areas between the nanowire and the implanted contact line were 2 µm at each side (outside the purple rectangular) create a total of 7 µm between source and drain. The opened passivation layer to define the gate area and to enable contact to the electrolyte solution was 13 µm in length between source and drain (blue rectangular) (figure 3.1, right). The nanowire surface was protected by dry oxidation of silicon, which resulted in a high quality gate oxide thickness between 6 nm to 10 nm depending on the fabrication process. The back gate contact to the bulk Si wafer was opened through the BOX layer by photolithography and wet etching. For the 16 × 16 and 32 × 32 arrays, the width of the wires was fixed to 500 nm (mask measure). For a more detailed description please refer to appendix A.

The purpose of the second sensor design was to integrate a micro fluidic cell to the chip and improve the device performances based on the results of the first run such as to eliminate the effect of the contact line resistance to the electronic characteristics of the devices, which will be discussed in section 3.2 and increase the sensitivity. The chips were designed in a 2 × 28 array of individual SiNWs having one drain contact each while sharing one common source. The layout of this second chip design is depicted in figure 3.2 (left). The wire lengths were varied (10 µm, 20 µm, or 40 µm, respectively) and the wire widths were either 200 nm or 400 nm (mask measures) from chip to chip. The implantation area of the source and drain contact lines were designed identically to the nanowire structure, while the gate opening was designed to be 2 µm larger than the implanted area on each side (figure 3.2, right). The pitch between the wires in a single line is 50 µm and between both lines it was 500 µm. The chip size was 7 × 7 mm enabling 100 chips on one 4 inch wafer. High density 128 × 128 arrays were included into this wafer design having a

pitch of 25 µm between all nanowires. The length and the width of the wires were 5 µm and 400 nm, respectively. Several test structures were added which will be described in appendix A

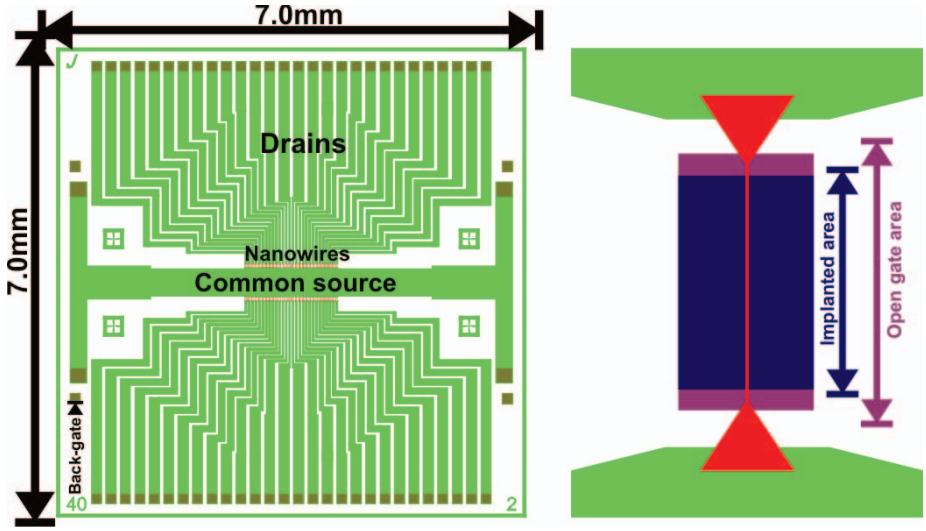

Figure 3.2. *The layout of the 2 × 28 SiNW sensor array (left) and the gate area with a single, individually addressable wire (right). Drain and source contact lines are shown in green. Grey parts are electrical contacts to the source, drain and back gate, respectively. Four mask alignment marks were added to the design to prevent the proximity effect of the nanoimprint process and further use for chip alignment. The source and drain contacts are highly ion implanted. The nanowire, which is a lowly doped p-type Si same as the original SOI wafer is shown in blue. The open gate area, which is 2 µm larger than the non-implanted area from each side, is shown in purple.*

3.1.2. Imprint mold fabrication

The nanoimprint mold (stamp) was fabricated by EBL and RIE on a 4" silicon wafer, too. In this process, a SiO_2 layer with thickness of 180 nm was thermally grown on the 4" silicon wafer by wet oxidation at 1050°C. Subsequently, a PMMA resist with a thickness of 230 nm was spin-coated onto the wafer (500 rpm / 30 s - 4000 rpm / 30 s) and then prebaked for 2 minutes at 180°C on the hot plate. The designed structures were transferred to the PMMA resist by direct e-beam writing with an e-beam lithography machine (Leica EBPG 5000 Plus). The electron beam writing processes were done in two steps. First the contact lines were defined and then the nanowires were defined with different parameters as shown in table 3.1 for the first run (the 4 × 4 arrays) and in table 3.2 for the second run

(2 × 28 arrays with single SiNW), respectively. These parameters were chosen from several e-beam dose tests performed to find out the optimized parameter for this "nano-microstructures" combination on the nanoimprint mold.

E - beam parameter / Structure	Dose (uC/cm2)	e-beam current (nA)	Beam step size (nm)
Conducting lane	250	250	50
Nanowire	250	1	5

Table 3.1 *The e-beam lithography parameters used for fabrication of the first nanoimprint mold*

E - beam parameter / Structure	Dose (uC/cm2)	e-beam current (nA)	Beam step size (nm)
Conducting lane	200	150	50
Nanowire	350	1	10

Table 3.2: *The e-beam lithography parameters used for fabrication of the second nanoimprint mold*

	After development	After CHF3	After Oxygen plasma
Depth of structures (nm)	**230**	**215**	**170**

Table 3.3. *Depth profiles of the structures on the mold fabrication process after each process steps*.

After electron beam writing processes, the PMMA resist was developed for 60 seconds in a developer solution (AR-600-55) with mega sonic support and then stopped in iso-propanol for 50 seconds. Because PMMA is a positive e- beam resist the areas that were subjected to the e-beam was dissolved in the developer solution and exposed the SiO_2 layer against PMMA. In the next step, the SiO_2 layer was etched by RIE using CHF_3 plasma (200 W, -500 kV). The etch stop was controlled using a laser interference signal. To ensure uniformity of the structures the etching process was over-etched for 45 seconds. The remaining PMMA resist was etched by oxygen plasma in the RIE. The depth profiles of

the mold, measured after each step, are summarized in table 3.3. The structures on the wafer were 170 nm in height, which was equivalent to the thickness of the SiO_2 layer. The roughness at the edges of the structures was in the range of 10 nm (figure 3.3)

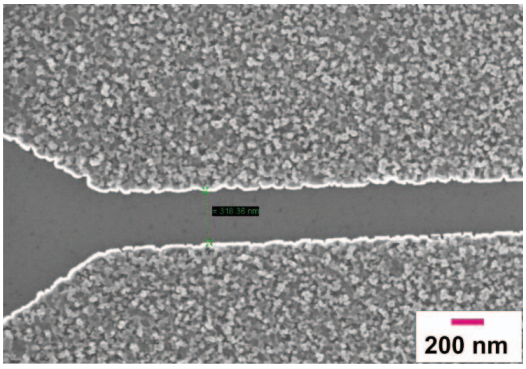

Figure 3.3. *SEM image of a wire structure out of the second imprint mold. The roughness at the border of the structures was in the range of 10nm*

In the final step, a monolayer of fluorsilane (Trichloro(1*H*,1*H*,2*H*,2*H*-perfluorooctyl) silane) was deposited on the wafer as an anti-adhesion layer to prevent sticking of the imprint resist into the mold during the nanoimprint process. The process was carried out by cleaning the wafer in acetone and iso-propanol and subsequently by Piranha solution. A surface activation process by oxygen plasma and subsequent gas-phase silanization was carried out in a glove box [155]. Successful silanization of the mold was confirmed by water contact angle measurements ($95^o \pm 5^o$), indicating that the surface was homogenously covered by the fluorsilane. It is noted that the anti-adhesion layer is very stable on the surface of the mold, which allowed many subsequent imprint processes at high temperatures including standard cleaning procedures in acetone and final ultrasonification.

3.1.3. Chip processing

Figure 3.4 depicts the main fabrication steps for the wafer-scale “top down” fabrication for SiNW sensor arrays on an SOI wafer. The process started by thinning out the SOI wafer and then growth of a thin layer of dry oxide on top of the SOI wafer, which was used as a hard mask. Then the nanoimprint lithography followed to define the contact lines and wire structures. Following the imprint, dry etching of SiO_2 by RIE and anisotropic etching of Si by TMAH solution were performed. Optical lithography and LPCVD techniques were employed for further chip processing and stable passivation of the devices against

electrolyte solutions. The imprint mold, all the masks for optical lithography and the final devices were fabricated at the clean room facilities of the IBN.

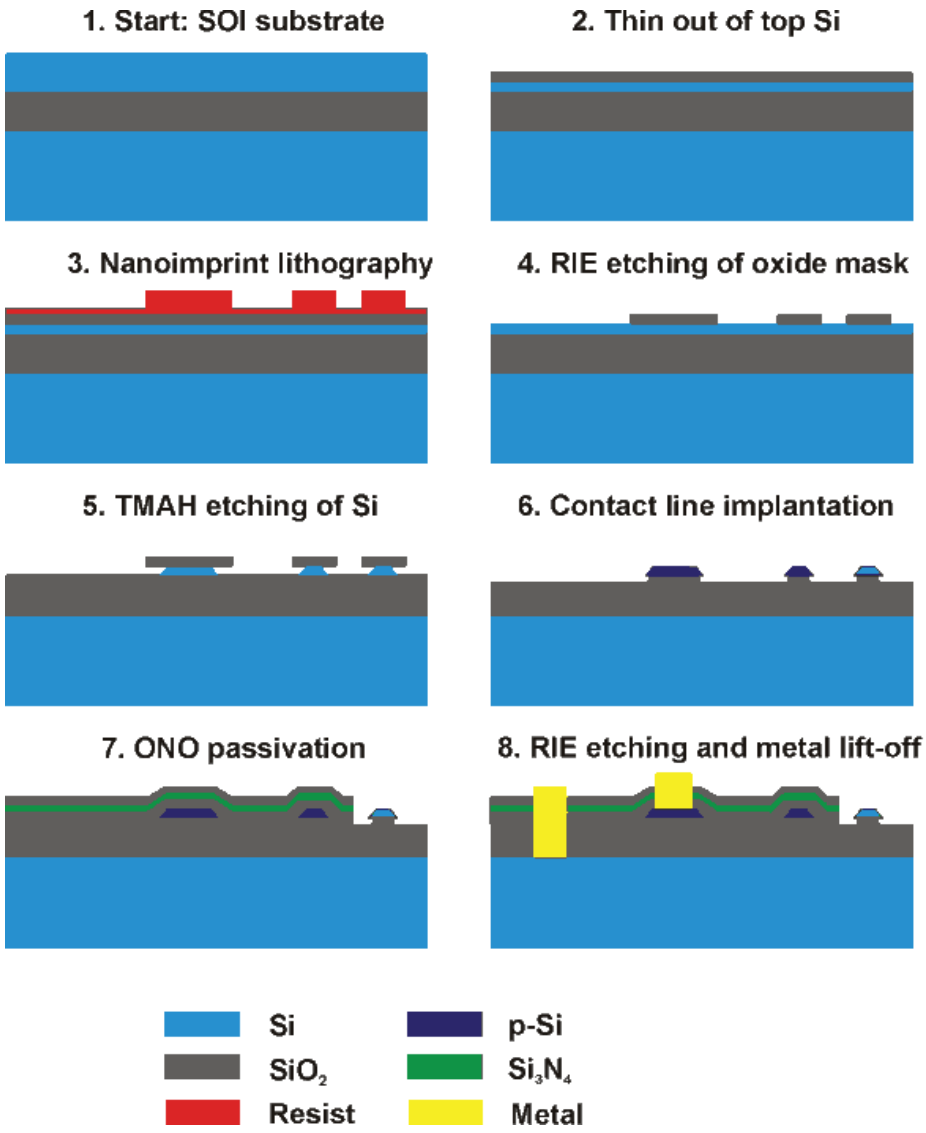

Figure 3.4. *Flowchart for the fabrication of the SiNW arrays. Our wafer-scale process for 4" SOI-wafers is combining nanoimprint lithography with wet etching of Si using TMAH. Contact lines are p-doped for reliable operation of the devices. The finalized structure in step 8 shows back gate contact, bond pad, contact line and open wire (from left to right).*

In the following, the fabrication steps of the nanowire sensors are described in detail:
"Unibond" silicon-on-insulator (SOI) wafers, purchased from SOITEC, France, were used as a starting material for the process (figure 3.4, step 1). The SOI wafers consisted of three parts: A buried oxide (BOX) layer, which had a thickness of 400 nm, in between a top Si layer (device layer), which had a thickness of 360 nm, and a Si substrate (handle wafer). The device layer and the handle wafer were boron-doped (p-type Si <100> with resistivity of 14÷22 Ωcm). The SOI wafers were firstly thinned out to achieve the desired thickness of the top Si layer by wet oxidation and wet etching. After that, a thin layer of dry, thermal oxide was grown as a hard mask layer for the TMAH etch step (figure 3.4, step 2). The detail parameters of the thinning down SOI wafer is given in appendix A.2. The consumed thickness of the Si device layer by the oxidation step was roughly estimated by following equation:

$$t_{Si} = 0.44 \cdot t_{SiO_2} \qquad 3.1$$

(t_{SiO_2} is the thickness of SiO_2 after oxidation and t_{Si} is the thickness of consumed Si for oxidation) [83].
Thermal nanoimprint lithography (NIL) transferred the structures from the mold to the SOI wafer (step 3). The nanoimprint process was performed by using an NX-2000, Full-Wafer Universal imprinter, with patented Air Cushion Press for ultimate nanoimprint uniformity by Nanonex. Inc. The imprint process was performed as described below:

- The nanoimprint resist (Nanonex 2010) was coated on the SOI wafer and incubated at 90°C for 20 minutes. The thickness of the resists was determined to about 220 nm by ellipsometry.
- The mold was cleaned in acetone with megasonic support and dried by Ar-gas. The SOI wafer and the mold were carefully aligned based on the large flat of the wafers and both were fixed by two polyester foils and transferred to the imprinter. The alignment had to be carried out carefully in order to have reliable devices, because the TMAH etching strongly depends on alignment of the structures with respect to the <110> direction. Before imprinting on the SOI wafers, the imprint was done on a test wafer to remove the small particles on the mold because a small particle will create a large defect on the wafer after imprint.
- The imprint chamber was evacuated for 5 minutes to remove air out of the structured cavities. After evacuation, the temperature of the imprint chamber was increased to 140°C and a pressure of 200 Psi was applied as the pre-imprint

process. The main imprint process was carried out at a temperature of 170°C and a pressure of 450 Psi for 6 minutes, which is the maximum processing time for thermal imprint of the imprinter. During the main process, the temperature and pressure were kept constant. After the main process, the imprint chamber was cooled down to a venting temperature of 40°C, while the pressure was kept at 450 Psi. When the temperature reached the venting temperature, the pressure of the imprint chamber was released. The mold and the substrate were carefully separated by hand at room temperature. The temperature and the pressure profile of the process are depicted in figure 2.11 (subsection 2.3.1).

As already discussed in section 2.3.1, the nanoimprint process relies on the deformation of the polymer layer and the structure transfer by imprinting creates differences of surface topography in the imprint polymer. To gain an access to the SiO_2 hard mask layer, the residual resist layer has to be removed by a further RIE step. In this step, the whole wafer surface was exposed to the oxygen plasma until the residual layer was completely removed. This step is very important in our process. Due to inherent inhomogeneity of the residual layer, this etching step represents an equalizing step. Details of this step will be discussed later. In our process, the residual layer was etched in oxygen plasma (O_2, 200W, 30 ccm) by RIE with a time variation in the range of a few seconds.

In step 4, the structures were transferred to the SiO_2 layer by RIE (CHF_3, 200W, 20 ccm). The etch stop was observed by a peak that appeared in the signal of the laser interference device of the RIE. Past to this signal, an over etching of 30 seconds was carried out. After that, the resist was completely removed by oxygen plasma. It has to be noted that for this step, the selectivity between the SiO_2 and the thermal imprint resist is very poor with a ratio close to 1:1.

In step 5, the TMAH etching was performed with a 25% TMAH solution, while the temperature was kept stable at 90°C during the process. Some previous studies showed the effect of the parameters concentration, time and temperature on the etching process. A higher concentration roughened the surface to a lesser extent [150]. Directly before the etching in TMAH solution, the wafers were dipped for 30 seconds into 1% HF solution to remove the native oxide. Then they were rinsed in deionized water. The timing of this step had to be kept constant for all the wafers, because the size of the final SiNWs depended on the size of the nanostructured SiO_2 hard mask. The Si was etched down to the BOX layer in about 15 seconds as observed by a change of the wafer color. However to ensure the process and to create smoothness edges of SiNWs, the wafers were etched for 1 minute and

were subsequently rinsed several times in deionized water. Figure 3.5 shows a SiNW after TMAH etching with the SiO_2 hard mask still on top. The top surface of the SiNW is defined as the dark shadow in the SEM image on the right. It can clearly be seen that the roughness at the edges of the SiO_2 hard-mask was not transferred to the SiNW structure during the TMAH etching step. It was rather found that the TMAH etching resulted in very smooth Si surfaces although the quality of the mold structure was not very good. This is one of the strengths of this fabrication protocol. On the transition part between the nano- and the microstructures, the etching rate was much faster than on the nanowire itself. The reason is that at this position other Si planes were exposed to the TMAH solution (picture on the left).

After the TMAH etching process, in the first process run, the oxide mask layer was completely removed by 1% HF solution and 50 nm of SiO_2 was deposited by low-pressure chemical vapor deposition (LPCVD). The LPCVD oxide on the contact lines was removed by optical lithography and subsequent wet etching (HF 1%). The oxide and the resist on the nanowire structures were left as protection mask for the feed line implantation. For the second process run, the oxide hard mask was removed only on the feed lines, while it remained on the wires. Here this oxide hard mask acted, together with the photo resist, as protection mask for the ion-implantation.

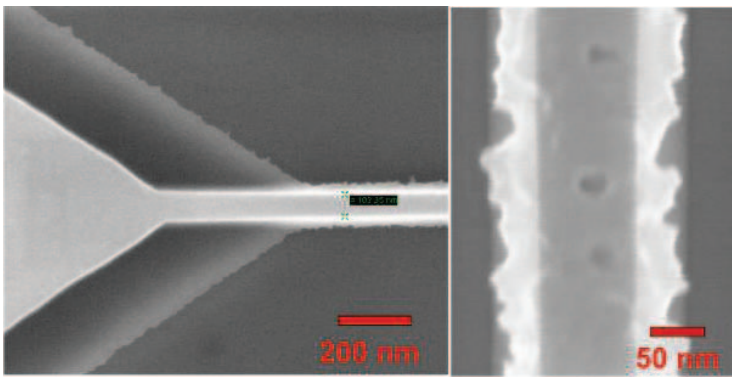

Figure 3.5. *Nanowire structure (transition part between nano- and microstructures) after TMAH etching. The silicon oxide hard mask can be seen on top. The TMAH etching process eliminates the roughness of the structure.*

In the following implantation step, boron ions were implanted on the contact lines to decrease the source and drain serial resistances of the SiNW arrays (step 6). The parameters were chosen based on simulation results (SRIM 2008). In the first process run, the boron ions were implanted with a dose of $5\times10^{14}/cm^2$ and an energy of 7 keV, while in

the second process run a higher dose of boron ions (1×10^{15}/ cm^2) was implanted with a lower energy of 6 keV . After the implantation, the photo resist was removed by acetone and the protection oxide layer was etched off by 1% HF solution. The wafers were then cleaned by a standard RCA process and subsequently annealed at 900°C for 30 minutes under the N_2 atmosphere to activate the implanted ions and restore mobility and other material parameters [83].

In step 7, the wafers were covered with a layer of high quality SiO_2 by LPCVD process (360 nm) for passivation of the contact lines against the electrolyte. In the second fabrication process, a thin layer of dry thermal silicon oxide (6 nm) was grown before LPCVD deposition to avoid a direct contact of the LPCVD silicon oxide to the SiNW surface.

The wafers were then structured by optical lithography and the LPCVD SiO_2 layer was etched with HF 1% to open gate areas (SiNW), source, and drain, and back gate contact pads. After that, standard RCA recipes were applied to clean the wafers. Then a dry oxidation process (820°C, 40 min) was performed to grow a thin layer of high quality oxide as gate dielectrics. Subsequently, the oxide on the contact pads was removed by an additional lithography and wet etching (HF 1%).

In the last step of the fabrication process, a lift-off process was performed to deposit a stack of metals (150 nm Al, 10 nm Ti, 200 nm Au) on the contact pads (Pfeiffer PLS 500 e-beam evaporator). Furthermore, a rapid thermal annealing step (RTA) (N_2-gas, 450°C, 10 min) was performed to form *ohmic* contacts.

3.2. Chip packaging and microfluidic fabrication

The chips were packaged or encapsulated to enable stable and reliable experiments in liquid environment. The encapsulation methods used for the SiNW chips were adapted from two previous protocols for the ISFET chips: flip-chipping and wire bonding [9, 42, 153]. Flip-chip was done with the SiNW chip of the 4×4 array of the first chip design only, while the wire bonding protocol was used with both designs: the 4×4 arrays and the 28×2 array of the second design. Figure 3.6 present examples of encapsulated chips with flip-chip protocol (left) of a 4×4 arrays chip and wire-bonding protocol (right) of a 28×2 arrays. The following paragraphs will describe in details each protocol.

Flip-chip encapsulation

For flip-chipping, the 5 mm × 5 mm chips were cut from the fully processed wafer and then cleaned with acetone and isopropanol in order to remove the protection resist. Due to

the mechanical properties of the SiNW, the cleaning steps needed to avoid strong mechanic treatment like ultrasound or mechanical manipulation. The electrical contact between the bond pads on the chips and the carriers was formed by printing of a two-component conductive silver glue (Epo-Tek H20E-PFC, PolytecGmbH, Waldbronn, Germany) on the contact areas of the carrier using a screen printer (SP-002, Essemtec AG, Aesch, Switzerland). Then the chips were mounted to the back side of PCB carriers (WI-KA GmbH, Baesweiler, Germany) by flip-chipping using a precise X-Y positioning system (Fineplacer 96, Finetech GmbH & Co. KG, Berlin, Germany). The glue was cured at 150^{o}C for one hour. Followed by application of a two component under fill epoxy (Epo-Tek U300, Polytec) or epoxy resin (Epo-Tek 302-3M, Polytec) around the chip. Due to its viscous properties the epoxy was dragged between the chip and the carrier, thus insulating everything but the bond contacts electrically. The epoxy was cured at 150^{o}C for 1hour. Finally, a small glass ring was glued on the carrier to form an electrolyte reservoir.

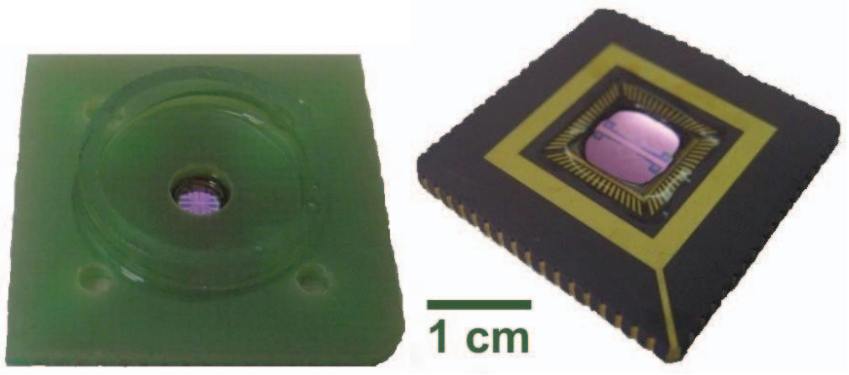

Figure 3.6. *Images of SiNW encapsulated chips by both methods: flip chipping (left) and wire bonding (right). The flip-chipping protocol was applied for 4×4 arrays chips while the wire-bonding protocol was applied mainly for the 28×2 arrays chips. With the second protocol, a microfluidic can be integrated on chip for analytes delivery.*

Wire-bonding encapsulation

For wire bonding the 7 mm × 7 mm chips were cut and cleaned as described above. Chips were fixed to a 68-pin LCC carrier (LCC 0850, spectrum, USA) by epoxy glue. An Al wire (Al/Si 1%, 25 µm -diameter, Müller Feindraht AG Switzerland) was bonded from the chip bond pads to the carrier via a wedge-wedge wire bonder. The epoxy resin or polydimethylsiloxan (PDMS) was manually filled on the chip to cover the bond wires and pads but still leave enough space for the micro fluidics (4.5 mm × 4.5 mm). The glue was cured at 80^{o}C for 3 hours (Epoxy) or at 150^{o}C for one hour (PDMS). A glass ring was

glued to the carrier and the space between the chips and the carrier was filled with the respective polymer used for the rest of the encapsulation. One has to consider the difference between the epoxy resin and the PDMS material. Epoxy is a stiffer and more stable encapsulation. Furthermore, it does not show significant swelling when in contact with electrolyte solution. However, it does not stand high temperatures (above 80°C) because above this temperature the epoxy melts and can be burned by H_2SO_4 (20%). In case of the PDMS encapsulated chips one has to be very careful to avoid the PDMS create a very thin film on the chip surface that is hard to remove after the curing process. Figure 3.6 presents an example of an encapsulated chip with the two discussed encapsulation protocols.

Microfluidic fabrication

The microfluidic structure was fabricated based on PDMS (Sylgard® 184, Dow Corning, Germany). First, the mold was mechanically fabricated by creating the reverse structure in an AlMg alloy. The structure consisted of two parallel channels (200 µm width and height) with two separated inlets and one common outlet. Second, the PDMS mixture (10:1) was filled into the mold and cured for 1 hour at 120°C. After removal from the mold, the PDMS structure was connected to a transparent external flow cell, which can be aligned to the chip surface and subsequently be fixed to the chip holder socket.

3.3. Measurement setup and electronic characterizations

The SiNW chips were characterized with respect to their electronic properties and to the measurement configuration for biomolecular sensing applications. Figure 3.7 schematically shows the measurement principle for SiNW devices. Generally, as discussed in section 2.1, the main features of SiNW FETs can be determined by the transfer characteristics and the output characteristics at room temperature. The transfer characteristics shows the drain current (I_{DS}) of the SiNW as a function of the gate-source voltage at constant drain-source voltages. The output characteristics show I_{DS} as a function of the drain-source voltage at constant gate voltages.

As can be seen in figure 3.7, the SiNW are surrounded by the high quality, thermally grown gate oxide (6-8 nm) that isolate the SiNW from the electrolyte and a BOX layer (400 nm) separating the SiNW from the handle wafer. Hence, the concentration of charge carriers in the nanowire can be controlled by an electric potential that can either be applied from the top through the thin oxide layer or from the bottom through the thick BOX layer. The first gate is the so-called front gate (FG), while the second is called back gate (BG).

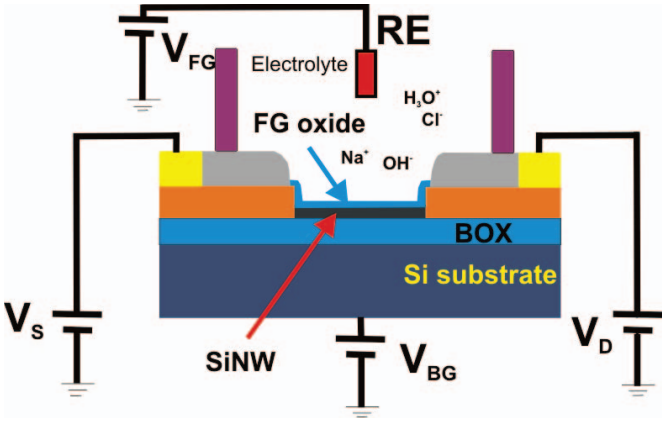

Figure 3.7. *Schematic illustration of the measurement setup for the characterization of the SiNW sensor arrays. A characterization using the back-gate can be done by applying the gate voltage through the Si substrate with the BOX layer as gate oxide. The front-gate characterization can be done by applying the gate voltage through the reference electrode immersed into an electrolyte solution.*

In this work, the thickness of the Si layer was 40-60 nm. At room temperature and under the assumption that no fixed oxide charges exist, the Si layer is fully depleted of charge carriers in thermal equilibrium [84]. Like in any SOI-fully- depleted device with such a thin top silicon layer, both gates are strongly coupled electrostatically. This is indicating that the back-gate potential affects the front-gate characteristics and vice versa [129, 156, 157].

For the front-gate characterization, the use of a suitable reference electrode is crucial to keep the electrochemical potential drop over the electrode-electrolyte interface stable, hence to keep the electrochemical potential of the solution stable. Therefore, a reference electrode (SUPER–DRI-REF, World Precision Instruments, USA) was used for all the front-gate measurements in this thesis. The characterization measurements were performed in a Titrisol buffer solution of pH 7. The back gate characterization was carried out either with or without electrolyte on the front oxide.

Two measurement systems were used throughout this thesis. They are shown in figures 3.8 and 3.9, respectively. Figure 3.8 shows the measurement setup that uses a commercial Keithley semiconductor characterization system (Keithley 4200 SCM), which has three source measurement units (SMUs) with variable potential and one which is connected to ground. The encapsulated chips were placed in the socket and connected to the system in

the following manner: The common source was connected to ground, while drain, front gate and back gate were connected to the SMU 1, SMU 2, and SMU 3, respectively. Figure 3.9 shows the custom-made amplifier system for the parallel characterization of multiple SiNW devices. The amplifier is a modification of an existing measuring system [42, 158]. In order to account for the smaller currents of the SiNW transistors, the feedback resistance was changed to 500 kOhm. The setup can measure the *dc* characteristics or the impedimetric response of SiNW by means of the transfer function of 16 channels simultaneously.

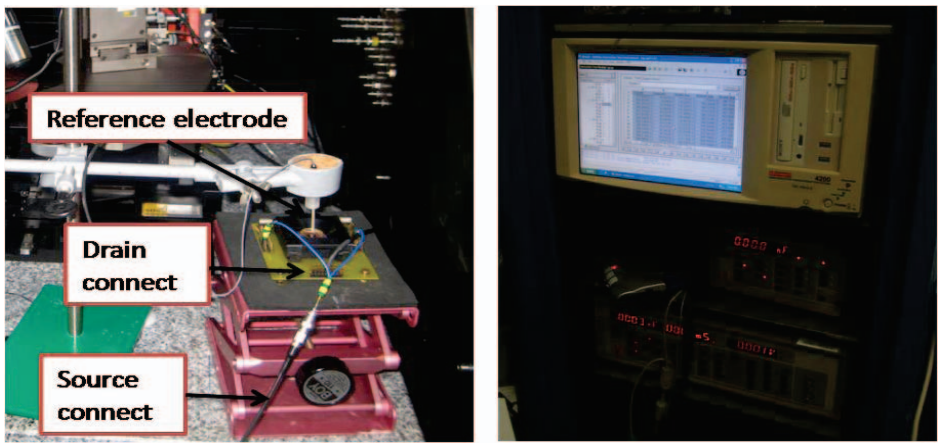

Figure 3.8. *Photographs of the measurement setup based on the Keithley 4200 SCM. The encapsulated chip is placed in a socket (see left image) and connected to the Keithley 4200 SCM (see right image). The source, drain, back gate and front gate are connected to the Keithley 4200 SCM by coaxial cables. The reference electrode was kept at a fixed position in all measurement.*

The back gate characterizations were carried out by applying V_{BG} from 30 V to -30 V. The V_{DS} was applied from -3 V to 3 V. The measurements were performed with or without the electrolyte solution at the front oxide to identify eventual influences.

The front-gate characterizations were carried out by applying V_{FG} from -3 V to 3 V and V_{DS} from -3 V to 3 V. In the case of the front gate, the reference electrode was used and kept at constant distance to the chip surface by an electrode holder.

The transfer characteristic was carried out by sweeping the gate voltage (V_{FG} or V_{BG}) forward and backward in the range of applied voltage, while the V_{DS} were kept constant. The output characteristic was measured by sweeping the V_{DS} at a constant gate voltage.

Transfer function characterization of the SiNWs was carried out by the readout setup shown in figure 3.9. The working point was set at the maximum transconductance of the transfer characteristics curves measured directly before the transfer function measurement. The frequency was applied from 1 Hz to 1 MHz with sinusoid signal amplitude of 10 mV through the reference electrode.

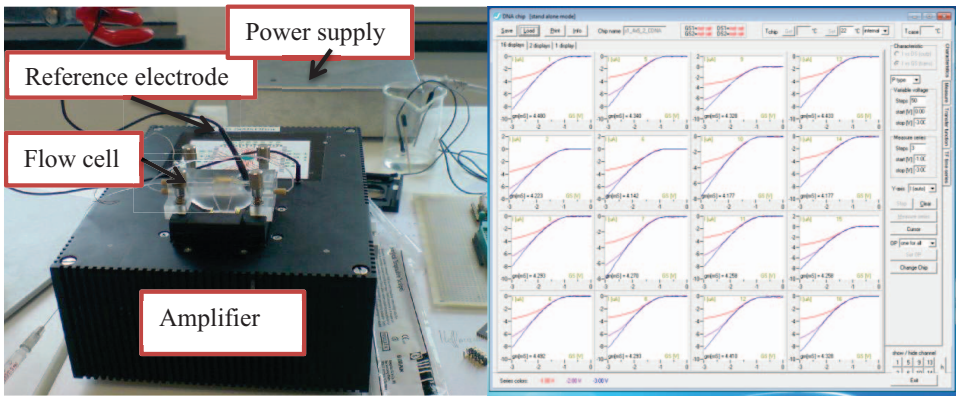

Figure 3.9. *Portable measurement setup using the custom-made 16 channel amplifier system and the software interface. The flow cell on top of the chip socket (see left image) can be removed for the experiment, if necessary. The amplifier in each channel has a feedback resistance of 500 kOhm*

3.4. Surface cleaning and modification for biomolecular binding

Chip cleaning

Cleaning the chip surface plays an important role for reliable experimental results, especially for the reused chips. The cleaning procedure needs to fulfill several requirements:

- The surface of the SiNW needs to be cleaned and still function properly.
- The electric properties need to be maintained after chip cleaning.
- The encapsulation must withstand the cleaning procedure.

In order to meet the above requirements, several tests have been performed to get the best procedures. The following paragraph describes the most stable procedure obtained by the tests.

The chips were encapsulated as described in section 3.2. The metal contacts were separated from the electrolyte by a polymer such as PDMS or medical epoxy. This polymer only withstands some chemicals. In order to avoid the effect of the oxygen plasma cleaning to

the electronic properties of the SiNW as discussed later in section 4.2, all the cleaning and activation steps for the chips were carried out by wet cleaning methods. One has to consider that the mechanical properties of the SiNW are not like the planar ISFET ones, so that the cleaning procedure has to avoid strong mechanic treatments such as ultrasonic or mechanical cleaning by cotton bud like in some procedures described for the MEAs or planar ISFETs [42, 159].

First, the encapsulated chip was rinsed with deionized water and in a second step cleaned with Piranha solution (2 H_2SO_4: 1 H_2O_2). The Piranha solution cleans contaminated organic molecules such as DNA, protein or silane molecules bound to the SiO_2 surface. Only a small drop of piranha solution was put on the center of the chip to avoid direct contact with the encapsulation materials. Then the chips were heated to 60°C for 10 minutes. In order to avoid the vapor from the piranha solution, this experiment has to be done in fume hut with a protection. In the next step, the chip was rinsed under a flow of deionized water for 5 minutes. Then the SiNW chip was cleaned with the Hellmanex 2% (HellmanexII, Hellma GmbH, Muellheim, Germany) at 40°C for 10 minutes and finally rinsed by deionized water for 5 minutes. One has to consider that the Hellmanex solution is an alkaline solution and also etches the silicon oxide. The etching rate of SiO_2 is increasing with increasing temperature and concentration. In some cases, the gate SiO_2 was etched away and consequently the SiNW was also etched by the Hellmanex solution. After cleaning, the surface was activated by applying a mixed solution of HCl: MeOH (v/v) at room temperature for 30 minutes in order to form the OH group at the SiO_2 surface needed for silanization. After rinsing with deionized water and drying with the Ar gas, the chips were directly transferred to the silanization process.

The effect of the cleaning procedure was also investigated by measuring the front-gate transfer characteristics of the SiNW chips before and after cleaning. For instance, the effect of plasma cleaning on the electronic properties of the SiNW and the long-term stability of the signal in the electrolyte solution were measured.

Surface functionalization

In order to have a reliable binding of the biomolecular probes to the oxide surface, the SiO_2 needs to be functionalized with a functional catcher molecule, which can be covalently bound to SiO_2 and exposes a functional group for further binding with probe molecules. For the DNA immobilization and protein binding, APTES and GPTES were normally used. The APTES silanization results in an amino-terminated gate that can further bind OH-terminated functional molecule. The GPTES silanization results in an epoxy-group

termination. The epoxy group then can be broken in a solution environment of pH 8-9 or by UV light illumination. The opening of the epoxy group leads to an OH-terminated surface that can further bind amino-terminated functional molecules. Figure 3.10 illustrates the APTES and GPTES silanization reaction with the SiO_2 surface.

In the experiments in this thesis, the silanization of both chemicals mentioned above was performed as follows: The freshly cleaned and activated chip was placed in desiccator containing 100 µl of silane molecule solution. After sealing of the desiccators, the chamber was evacuated for one hour. The pressure of the chamber was adjusted to 5mbar for APTES and 45 mbar for GPTES silanization. The silane fume spread over the desiccator and created a homogenous monolayer of silane on the chip surface [42, 88]. The GPTES silane layer was in the range of 1 nm [88]. The water contact angles measured after the silanization were 60^o for the APTES silanization and $66^o \div 70^o$ for the GPTES silanization, respectively, indicating that the silane molecules were bound to the surface.

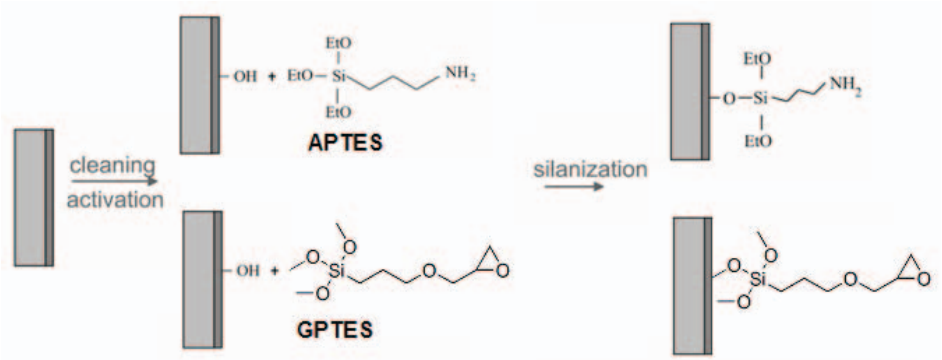

Figure 3.10. *Schematic drawing of the gas-phase silanization reaction between the gate oxide and the APTES, which results in an amino-terminated surface, and GPTES, which results in an OH-terminated surface.*

3.5. pH sensitivity experiments

As discussed in section 2.2, the *amphoretic* groups at the oxide surface can be protonated or deprotonated depending on the pH value of the bulk solution according to the site binding model. The protonation and deprotonation of the *amphoretic* group at the oxide surface relates to the change of the surface potential according to Nernstrian equation 2.13. This change of the surface potential at the gate oxide interface causes the change of the flat-band voltage according to equation 2.1. In an ideal case, the change of the surface potential, called the Nernstrian response, is approximately 59.3 mV/pH. With a silicon

oxide surface, a value of about 30-40 mV/pH is achieved, depending on the cleaning status [94].

Generally, the standard open-gate FETs of our group can be used to detect the pH of the solution by observing the change of the output signal of these devices, when the pH of the solution changes. In this thesis, the pH sensitivity of the SiNW - FETs was investigated by different measurement techniques: i) The change in the transfer characteristics and output characteristic as a function of pH values, ii) The change of the current I_{DS} to the change of the pH value of the solution at a certain working point (V_{DS} and V_{FG} are constant).

All pH experiments with SiNWs were carried out with the Titrisol buffer with a pH value ranging from 2 to 12. The chips were cleaned as described in section 3.4. The pH standard measurements were carried out on the bare and freshly cleaned SiO_2 without further surface modification.

3.6. Detection of Ca^{2+} ions by SiNWs

Ca^{2+}ions play an important role in eukaryotic cells. They are involved in signal pathways, induce neurotransmitter release and act as cofactor in the activation of enzymes and hormones. Calmodulin (CaM) is an acidic protein consisting of approximately 148 amino acids and four EF-hand motifs that are responsible for Ca^{2+} binding, when intracellular Ca^{2+} concentrations are elevated from a resting submicromolar level to a concentration one or two orders of magnitude higher [160]. Ca^{2+}-bound CaM activates various proteins that modulate physiological activities, including gene transcription, muscle contraction, and neurotransmitter release [161]. The binding of Ca^{2+} ions to the CaM is reversible and is a fast process. Sensors with CaM modification for the detection of Ca^{2+} ions in the biological environment give more information about the activity of biological processes such as muscle contraction, protein secretion, cell death, and development [162]. Previous studies employed the possibility that SiNWs can be used for highly sensitive detection of Ca^{2+} and CaM-interacting proteins [127, 163].

In our work, a part of the CaM peptide (shown in figure 3.11) was used for the purpose of Ca^{2+} ion detection. The peptide was covalently immobilized on the SiNW surface as following: The SiNW chips were cleaned and silanized with GPTES in a gas phase process as described above. 10 mM of CaM peptide in pure sodium phosphate buffer (150 mM, pH 8.5) was added on the chips surface and incubated for 2 hours. The amino group of the peptide reacts with the OH functional groups of GPTES to form a strong covalent bond between peptide and the SiNW surface. The chip was rinsed by the phosphate buffer and

then with deionized water. The measurement was carried out in a 0.01× PBS buffer. The Ca^{2+} ions were diluted in the 0.01× PBS buffer and added to the electrolyte during the electrical measurement to observe the interaction between Ca^{2+} and CaM peptide.

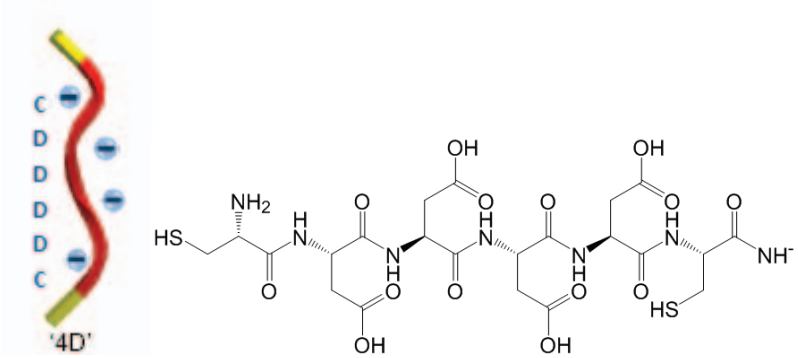

Figure 3.11. *Structures and chemical formula of the CaM peptide used in this work for Ca^{2+} detection* [164].

3.7. Polyelectrolytes multilayer build up on SiNWs devices

Polyelectrolytes (PEs) are polymer chains with repeating units of an electrolyte group. These groups will dissociate in aqueous solutions (water), leading to charged polymers. The polyelectrolyte properties are, thus, similar to both, electrolytes and polymers. The PEs show both characteristics of salts and polymers. This means that their solutions are electrically conductive and often viscous. These structures that are commonly present in soft matter systems play a fundamental role in determining structure, stability and the interactions of various molecular assemblies [165]. Many biological molecules are polyelectrolytes. For instance, polypeptides of protein molecules and DNA are polyelectrolytes.

PE multilayers on a substrate can be formed by alternating adsorption of polyanions and polycations in solution. For a first layer, a charged substrate is immersed into the PE solution with opposite charge to the surface for a certain time (2-20 minutes) followed by rinsing with the pure electrolyte buffer. The second layer is formed by immersing the substrate to the opposite charged PE solution followed by again rinsing with the buffer. This method is the so-called layer–by-layer self-assembly method which was introduced by Decher et al. [166]. This method has practically no limitations to build up multilayers on various substrates and can also be extended to a variety of charged materials such as nanoparticles, proteins, DNA [165, 167-170]. The main force contributing to the multilayer

formation is the electrostatic interaction between the negatively and positively charged polyanions and polycations, respectively. Besides, the contribution of other interactions such as hydrogen bonding and hydrophobic interaction can also influence the multilayer formation, however to a lesser extent.

The formations of the PE multilayer strongly depend on the salt concentration and the pH value of the dissolved PE solution rather than the concentration of the polyelectrolyte [165, 168]. Within the multilayer, the adjacent layers strongly interpenetrate with each other and the charges partly compensate each other [42]. For strong PE layers, one third of the charges combine with the previous layer. The remaining charge is compensated by counter ions and the following adsorption. The weak PE layers, the thickness and the surface coverage depend on the pH due to pH-depended swelling [42].

Multilayer adsorption of polyelectrolyte on field-effect transistors can be utilized as a model for biomolecular assays. Previous experiments employed multilayers of two differently charged polyelectrolytes on ISFET devices [42, 46, 82] or on electrolyte-insulator-semiconductor (EIS) structures [171] to model the charge based detection mechanism of biomolecules by these field-effect devices.

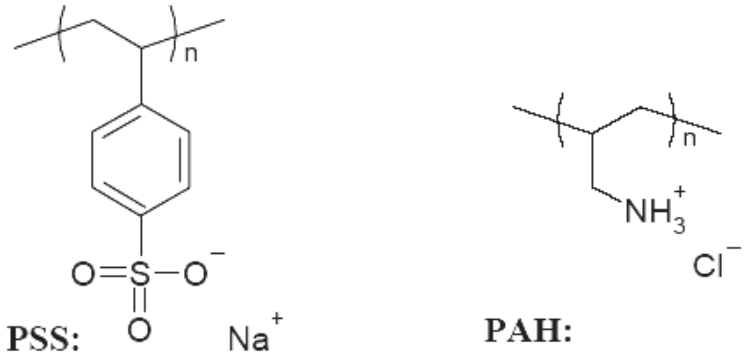

Figure 3.12. *Chemical formulas of PSS and PAH [42]. PSS is totally dissociated in aqueous solution and possess negatively charged molecule. PAH is positively charged molecule and the number of charge depend on the pH of the aqueous solution.*

In this work, poly (sodium 4-styrenesulfonate) (PSS) and poly (allylamine hydrochloride) (PAH) was used. The structures of the PSS and PAH are shown in figure 3.12, respectively. PSS is a strong polyanion that totally dissociates in aqueous solution. Therefore, it is fully negatively charged. PAH is a weak polyelectrolyte and it can only be

charged when dissolved in low or medium pH-value solutions. In high pH-value solution, the allylamine hydrochloride groups donate H^+ ions and form an uncharged amine group.

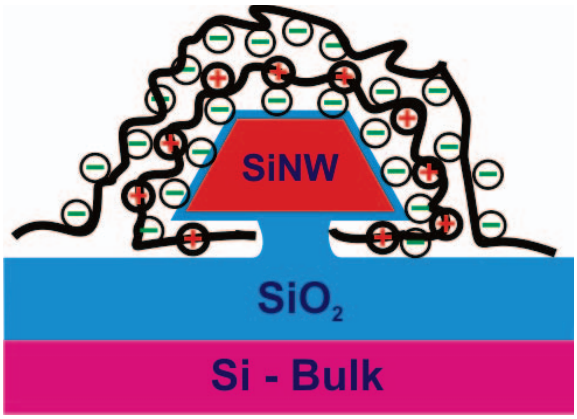

Figure 3.13. *Formation of a multilayer of PEs on the SiNW chips by electrostatic adsorption. First, the positively charged PAH polymer was adsorbed on the freshly cleaned, negatively charged SiO_2 surface. Repeated adsorption of oppositely charged PE layers resulted in a buildup of a PE multilayer.*

The potentiometric measurements of PAH/PSS multilayers on SiNWs was carried out by measuring the transfer characteristic of the SiNW after deposition of each layer. For this purpose, the chips were cleaned and activated by piranha solution at 60°C for 10 minutes. The PAH and PSS polyelectrolytes were diluted in 10 mM phosphate buffer and then the pH value was adjusted to 5.5 [171]. The concentration of the PEs were 50 µM for both PAH and PSS solution. The cleaned SiO_2 substrate was firstly immersed into the PAH solution for 20 minutes and then rinsed three times with the buffer solution. The electrostatic interaction between the negatively charged SiO_2 surface and the positively charged PAH forms the monolayer of the PAH on the SiO_2 surface. In the next step, the SiO_2/PAH substrate was immersed into the PSS solution for 20 minutes to form the SiO_2/PAH/PSS layers. Further layer by layer adsorption was achieved by cycle repetitions separated by repeated rinsing steps with the buffer solution. The transfer characteristics were measured after the rinsing steps to observe the output signal, respectively. For in situ measurements, the PE solutions were applied through the microfluidic chamber. The pure buffer was rinsed through the chamber in between each PE solution exchange to wash away the unbound PEs as well as to avoid agglomeration and precipitation of the PEs in the chamber. Figure 3.13 illustrates the formation of a PE multilayer on the SiNW

structure. The large surface to volume areas of the SiNW were covered by the layers of the PE molecules compared to the planar micro scale ISFETs.

3.8. Detection of biotin-streptavidin binding by SiNW

The biological affinity reaction between biotin and streptavidin was chosen to demonstrate the versatility of the SiNW biosensor. Biotin is a small, hydrophobic molecule that functions as a coenzyme of carboxylases. It is a naturally occurring vitamin found in every living cell. Streptavidin, a near-neutral, biotin-binding protein isolated from the culture medium of *Streptomyces avidinii*, is a tetrameric nonglycosylated analogue of avidin with a molecular weight of about 60,000 Dalton. The isoelectric point of streptavidin is 6.4 [172]. Streptavidin shows a negative charge when diluted in an electrolyte with a pH-value higher than the isoelectric point and positively charged when the pH-value is lower. The biotin and streptavidin binding is one of the strongest affinity reactions in nature [173] with a dissociation constant of $K_d \sim 10^{-15}$. The reaction is rapid and essentially non-reversible and the complexes are extremely stable over a wide range of temperature, pH, organic solvents and denaturing reagents. The high affinity of the biotin-streptavidin system has found applications in different fields of biotechnology including immunoassays, histochemistry, affinity chromatography, and drug delivery. Each streptavidin molecule has four biotin-binding sites. Typically, the streptavidin-biotin system is used for signal-amplifying "sandwich" complexes between specific reagents (e.g. antibodies) and detection reagents (e.g. fluorophores or enzymes). The specificity and detection reagents are independently conjugated, one with streptavidin and the other with biotin, or both with biotin, providing synthetic flexibility.

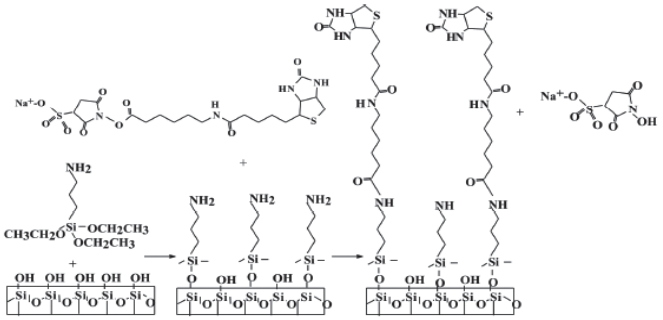

Figure 3.14. *Schematics for the reaction of EZ-Link Sulfo-NHS-LC-LC-biotin with an amino-terminated surface. This creates a covalent linkage of the biotin probe to the surface [42].*

The biotin layer on supporting substrates can be used as a binding site in the detection of anti-biotin antibodies or avidin/streptavidin tagged detectors. This binding serves as a model system for protein interactions as the binding process is well understood [173].

In this work, the SiO_2 surface was biotinylated by a covalent bond between the EZ-link Sulfo NHS-LC-LC biotin and the amino terminal group functional on the SiO_2 surface. EZ-Link Sulfo-NHS-LC-LC-biotin (sulfosuccinimidyl-6-[biotinamido]-6-hexanamido hexanoate) enables simple and efficient biotin labeling of antibodies, proteins and any other primary amine-containing macromolecules. The reaction principle of the biotin with the amino-terminated SiO_2 surface is depicted in figure 3.14. NHS-activated biotin reacts efficiently with primary amine groups in pH 7-9 buffers to form stable amide bonds [42, 174]. In practice, the chips were cleaned and modified by gas phase APTES silanization described in section 3.4. Biotin was immobilized on the SiNW surface by adding 20 µl of 0.5 mg/mL biotin in 10 mM boric acid (pH 8.5) to the chip followed by incubation for two hours [42]. The chips were rinsed with the same buffer several times and then rinsed with deionized water to remove unbound molecules. The electronic characterization of the transfer characteristics was carried out after each step. For biotin-streptavidin binding, the streptavidin was diluted in 0.01×PBS buffer and pipetted to the electrolyte solution during the real- time measurement. Figure 3.15 illustrates the biotin-streptavidin binding on the SiNW used in this work.

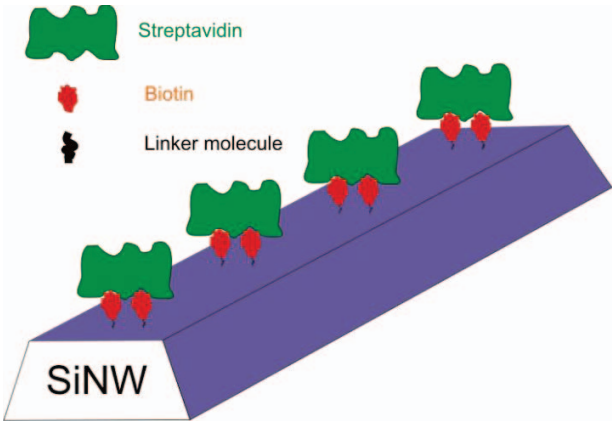

Figure 3.15. *Schematic of biotin-streptavidin binding to the SiNW surface. The gate oxide of SiNW was first modified with APTES. After that Biotin was covalently immobilized through the reaction shown in figure 3.14. Each streptavidin molecule binds to two biotin molecules on SiNW.*

3.9. Detection of DNA by SiNWs

DNA is a nucleic acid that contains the genetic instructions used in the development and functioning of all known living organisms and some viruses [175]. The main role of DNA molecules is the long-term storage of information. The DNA segments that carry this genetic information are called genes and are involved in regulating the use of this genetic information. DNA has a double helical structure [176] with two single strands of long polymers. A single strand contains a backbone build from sugar and phosphate groups and nucleotides base group attached to the backbone. The backbone is negatively charged due to the phosphate groups and the strands are held together by hydrogen bonds between nucleotides. There are four different types of nucleotides found in DNA. The four nucleotides are named: adenine (A), thymine (T), cytosine (C) and guanine (G).

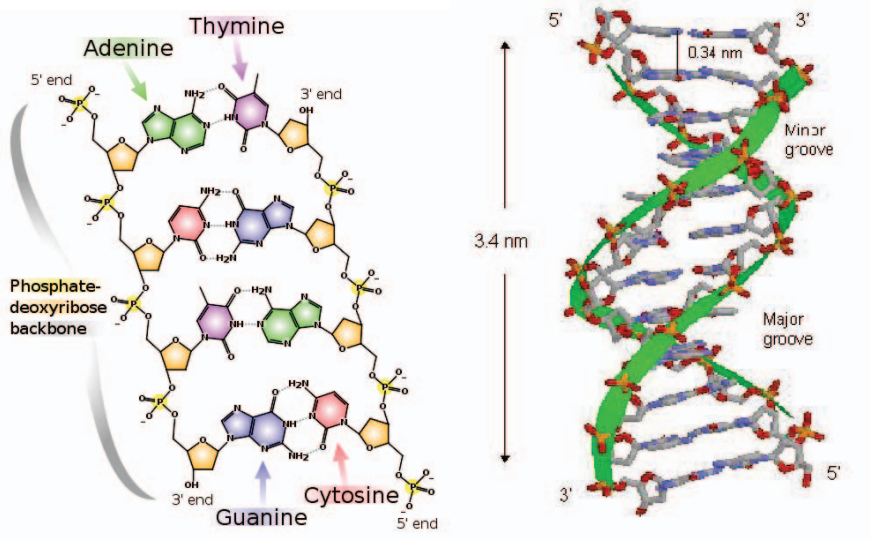

***Figure 3.16**. Chemical structure of a DNA and a double helix form [176]. The DNA double helix created by the single stranded DNA when it has matching between the nucleotides.*

The process of forming a double helix from two single-stranded DNA (ssDNA) molecules is called hybridization and is achieved by complementary paring of two base pairs (bp) via hydrogen bonds. The paring is not arbitrary, but only two pairs exist: A-T and G-C. A to T are connected via two hydrogen bonds and G to C via three hydrogen bonds. An important consequence of this pairing scheme is that a ssDNA molecule can combine only with its precisely fitting complement. This fact can be utilized for recognition of individual DNA molecules and individual organisms. For this purpose, a characteristic part of ssDNA is

immobilized at a surface and acts as a probe. The complementary strand DNA (cDNA) in the analyte is hybridized to the probe and forms a double stranded (dDNA).

The hybridization process of the DNA is strongly affected by the pH value, ionic strength of the solution, temperature. In addition, this process involves the formation of hydrogen bonds between two negatively charged strands. Therefore, parameters like probe sequence length, DNA concentration, and nucleotide sequence are also affecting the reaction.

Due to the electrostatic repulsion of the two ssDNA molecules, in higher salt concentration electrolyte, the DNA hybridization yield is higher and the double helix is more stable than in a lower salt concentration.

For DNA sensor applications, the immobilization of ssDNA on a solid support substrate plays an important role in DNA biosensor research. The immobilization can utilize the electrostatic interaction between negatively charged ssDNA on positively charged surfaces such as poly-L-Lysine on a SiO_2 surface [40, 52]. A more preferred method of immobilization of ssDNA to the substrate is a covalent bond via a cross linker reaction. The covalent binding has some advantages over the non-covalent binding, such as higher surface coverage, better orientation of the probes and a higher stability of the probe binding to the surface.

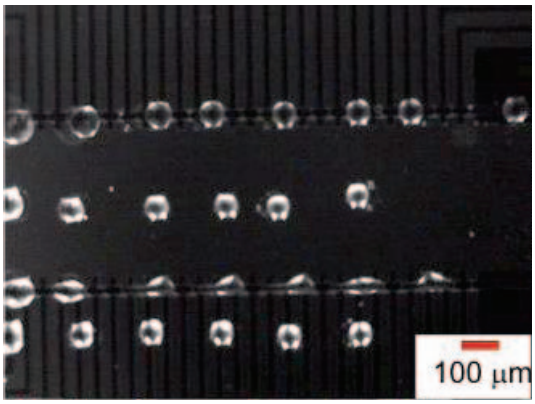

Figure 3.17. *Optical image of ssDNA solution was selectively spotted on the SiNW arrays and incubated at 37^0C for overnight.*

In this work, the ssDNA was immobilized to the SiNW surface by both methods. For electrostatic interaction, the SiNW surface was coated by poly-D-lysine (PDL), which is a positively charged molecule (20 µg/mL, 0.01×PBS). After that, ssDNA diluted in 0.01 × PBS buffer was added to the surface and incubated for 1 hour. The negatively charged ssDNA is undergoing an electrostatic interaction with the positive charge of the PDL layer

to form a layer of probe DNA on the surface. The DNA was added until the surface was saturated with ssDNA.

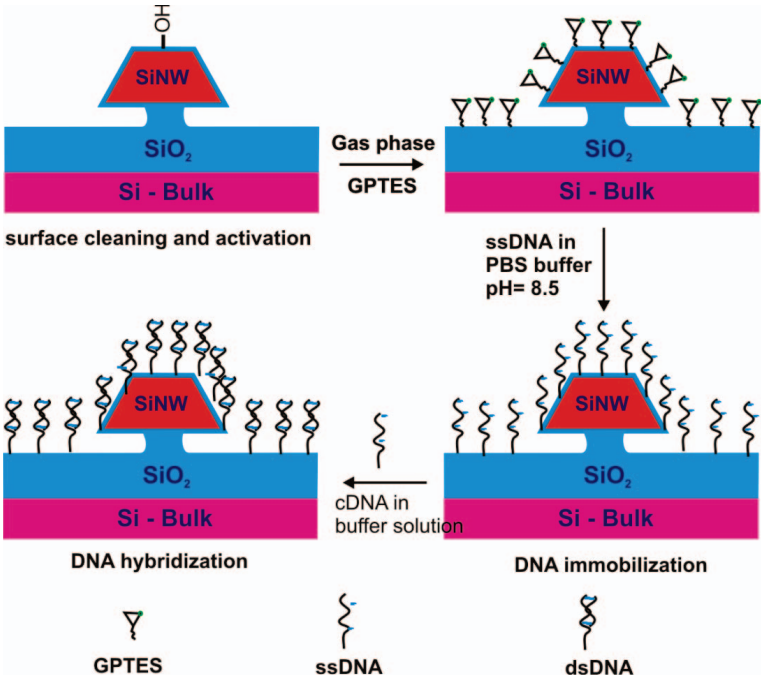

Figure 3.18. *Schematics illustrate the DNA immobilization and hybridization processes on the SiNW chips. In the first step, SiNW was cleaned and activated by wet chemical method. In the next step, the surface was gas-phase silanized by GPTES. The epoxy ring of GPTES molecules was opened in PBS buffer pH 8.5 and covalently binds to amino group of the amino-modified ssDNA. cDNA molecules in the buffer solution hybridized with the ssDNA-immobilized form double stranded DNA on the SiNWs.*

For covalent binding, the amino modified ssDNA was immobilized on the respective SiNW array. The chip surface was silanized by the gas phase GPTES process (section 3.4). The 20-nucleobases sequence of the probe DNA was 5'- amino C6-ATGAACACTGCATGTAGTCA-3'. The probe DNA was diluted in immobilized buffer, which was composed of 150 mM phosphate buffer, 0.5 M NaCl with a pH value of 8.5. The concentration of the probe DNA was 2 µM. The probe DNA solution was selectively spotted on the respective SiNW by a custom-made spotter system [158] and incubated at 37^0C for 2 hours or overnight. Each spot has about 0.5 nl of DNA solution. The humidity of the incubator helped to keep the spot in the same condition of pH and concentration during the immobilization process. Figure 3.17 shows the DNA spotted on the chip

surface. The reaction of the amino groups with the hydroxyl groups lead to a strong covalent bond of DNA on the SiNW. After the incubation time, the SiNW was rinsed by the same buffer several times in order to remove non-covalently bound DNA from the surface of the chip followed by a deionized step to remove the salt contamination from the immobilized solution.

The hybridization process was carried out in either ex-situ or in-situ experiments. In the ex-situ process, the target DNA (cDNA) was diluted in 1×SSC buffer solution with a concentration of 500 nM and added to the chip and incubated for two hours. After that the chip was rinsed with the same buffer and subsequently with deionized water. For the in-situ process, cDNA was diluted in 0.01×PBS buffer and was added to the chips during the electrical measurement.

The front-gate transfer characteristic of the chip was recorded within a low concentration of a diluted PBS buffer (diluted 100 times, 0.01xPBS) after each step. The in-situ measurement was carried out with the same buffer and at a maximum of transconductance of the SiNW. The DNA immobilization and hybridization on the SiNW surface is illustrated in figure 3.18

Chapter 4. Characterization of the SiNW devices

4.1. Structures and topography of the SiNW arrays

In the frame work of this thesis, two fabrication processes round of the SiNW sensor arrays on wafer-scaled was successfully established. A possible mass production as well as the reliability and reproducibility of the devices were demonstrated. For the complete fabrication process, nanoimprint lithography and wet anisotropic etching of Si by TMAH were established and included in the process flows for SiNW sensor fabrications at the clean room facilities of the IBN. In the second process run, several improvements over the first process run were achieved and will be discussed in this section.

First process run

Figure 4.1 shows a differential interference contrast (DIC) image (left) of a 4×4 array nanowire and a SEM image (right) of the topography at a sensing area of the 4×4 array chip from the first fabrication run. A single sensing area consisted of six SiNWs in parallel connected via source and drain contact lines. The opened area in the thick layer of LPCVD oxide passivation was 14×20 μm.

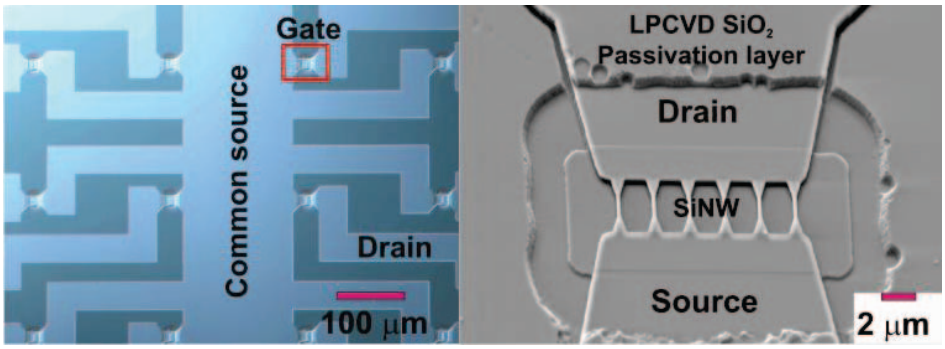

Figure 4.1. *DIC image of the 4×4 arrays of a finished chip out of the first design (left) and SEM image of one of the gate areas including six nanowires in parallel (right). The small gap between the contact line and the passivation layer was due to the non-perfect deposition of LPCVD on the vertical structure.*

Design (nm)	100	200	500	1000
Real (nm)	80±10	130±10	360±10	900±20

Table 4. 1. *The bottom widths of SiNWs after the wet etching process in TMAH (second row) compared to the widths of the wires in the initial design (first row). The variation is about 10÷20 nm.*

Geometry of the finalized-SiNWs were different and depend on the initial designed shapes. The length of the nanostructures depended on the wet etching time in TMAH as well. In our process the anisotropic etching of Si in the TMAH solution was 1 minute, therefore, the length of the wires was slightly longer compared to the initially designed structures. The width of the SiNWs was defined by the smallest width of the SiO_2 hard mask along the wire structure. Due to the roughness at the edges of the SiO_2 hard mask after the RIE process (Figure. 3.5), the size of the SiNWs after TMAH etching for the 200 nm design was 130 nm at the bottom width and 70 nm at the top width of the trapezoidal-shaped cross-sections. The size of the SiNW was determined by SEM characterization. The width of the wires had small variation from wire to wire and from chip to chip. It was mainly caused by the edges imperfection of the SiO_2 hard mask. For the smallest design with 100 nm wires, the wet etching process was not reliable. Some of these small wires were completely etched away in the TMAH solution due to the roughness of the SiO_2 hard masks. For the downsizing effect by wet etching two reasons added up. First, the imperfect transfer of the design to our custom made nanoimprint molds and, second, the transfer of

these structures to the SiO_2 hard mask by RIE etching. The bottom widths of the wires of the finished chips are summarized in table 4.1.

In figure 4.1 (right), small gaps between the contact lines and the passivation layer are visible. The reason was that the LPCVD oxide layer at the vertical walls was thinner compared to this at the planar surfaces. This effect was caused by an over etching of the SiO_2 layer during the gate opening process, which resulted in an extended etching along this interface.

From the SEM image in figure 4.2 (left), it can be seen that the SiNWs at the final stage of the process is much rougher compared to the very smooth surfaces of the SiNWs after the TMAH etching. The reason for this is the two step passivation procedure using an LPCVD deposition on the wires, one as protection for the ion implantation and another one for the final passivation layer. Both LPCVD layers were deposited, in the first process run, directly on the Si surface. These two steps resulted in defects on the surfaces, which lead to an increase of the surface roughness.

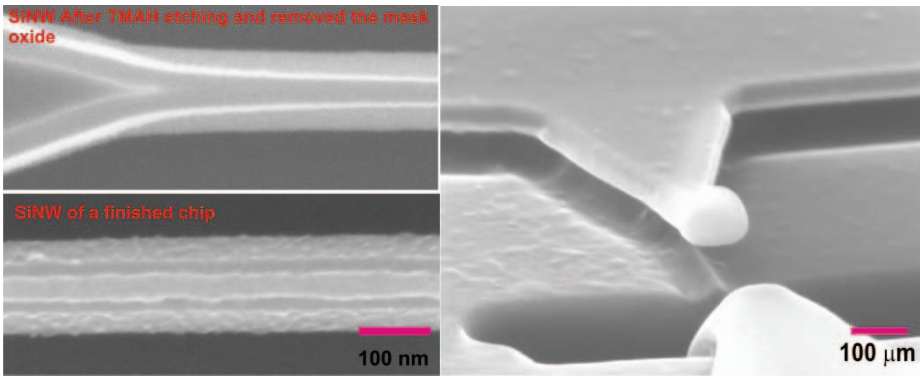

***Figure 4.2**. SEM image of the SiNW surface after TMAH etching (upper left) and of a finished chip (lower left). A cross section of a 130 nm SiNW (size in width at the bottom) is prepared by focus ion beam cutting (FIB) (right). It can be seen that the small nanowires became free standing due to the over etching of the BOX during the processes.*

The cross-section of the nanowires was studied after performing a focus ion beam (FIB) cutting as shown in figure 4.2 (right)). The results revealed that the small wires (130 nm) were free standing. The reason for this was the over etching of the BOX layer during the removal of the mask oxide after TMAH etching. In this step the oxide of the BOX was also etched to a same amount as the oxide hard mask and was laterally removed underneath both sides the SiNWs with roughly 80 nm at each side. This over etching side effect became more serious with each proceeding oxide etching step. The thickness of the top Si

layer on the chips was only around 50 nm, which was also measured by the SEM images of the FIB cut samples.

Second process run

In comparison to the first process run, the second process was improved in certain steps of the process flow. Firstly, the chips design was considered to have a better distribution of the structures as well as some additional cavities, which were added at the less dense areas, as it can be seen in between the common source and drains in the 4 corners (figure 3.2, chip design). The individual drain contact lines were designed in a way that the distribution of the imprint resist was resulting in a homogenous residual layer after imprinting, while still guaranteeing the same resistances of the drain contacts. The mask oxide layer had a thickness of only 30÷50 nm, which was much thinner than in the first process run. For the ion implantation, directly the mask oxide and the photo resist were used as passivation layers. Before depositing of the LPCVD SiO_2 layer for passivation, a thin layer of oxide was thermally grown on top of the Si structures to avoid the LPCVD oxide being directly deposited onto the Si. The passivation layer was thicker than in the first process run to improve the coverage of the passivation layer especially at the high step edges between the contact lines and the down etched areas. In this second design the SiNWs were arranged in two parallel lines, which enabled an easy integration of the chips with an external PDMS microfluidic system. In future processes, micro- or nanofluidic channels could be directly integrated into the fabrication process.

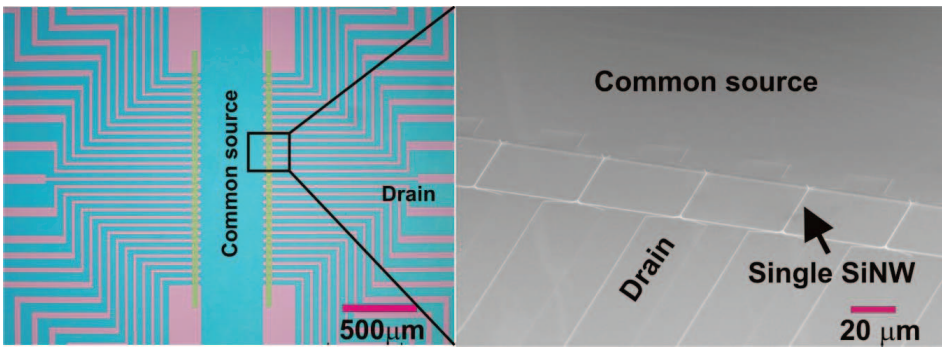

Figure 4.3. *DIC image of the 2×28 sensor array of the second chip design at the center of a finished chip (left) showing the planar SiNW arrays. SEM image of a closer view (right), showing the individually addressable SiNWs between the drain contacts and the common source contact.*

A DIC image of a finally processed chip out of the second process run is shown in figure 4.3 (left) and the SEM image with a closer view is shown in figure 4.3 (right), respectively.

In this process, nanowires with different length ranging from 10 µm to 40 µm were produced. The widths of the wire were proportional to the total etching time in TMAH. The etching rate of Si (111) in our protocol was approximately 18 nm/min. With 5 min etching time in TMAH solution, we were able to tune the widths of the wires from 200 nm down to 60 nm with lengths up to 40 µm and a very high reproducibility from wire to wire on the wafer. However due to the under etching of the SiO_2 explained before, the thinner wires were free-standing after removal of the oxide hard mask. Since during the complete process the wafer had to undergo many process steps, some of these thinner wire structures were broken.

Lengths / Widths	10 µm	20 µm	40 µm
200 nm	155±10 nm	120±10 nm	120±10 nm
400 nm	330±10 nm	300±10 nm	270±10 nm

***Table 4.2**. The bottom widths of SiNWs (in nm) of the second process run in relation to the widths of the wire in the design. The variation was approximately 10 nm. The Si thickness was 44÷55 nm.*

Also shorter wires were more stable than longer ones. Especially during the different cleaning steps in a process run the longer and thinner wires tend to break. The sizes of the final wires on the wafers of the second process run measured by SEM are summarized in table 4.2. The variation of the wires widths on a whole wafer was about 10 nm. The surface topography of the chip was highly improved compared to the first process run (figure 4.4). The SiNWs were arranged periodically on the flat surface of the large gate areas in between the open area of the high quality LPCVD oxide contact line passivation layer (figure 4.3, left; figure 4.4, left). This will prevent any vortex of the analyte solution inside the small micro fluidic channel and will result in laminar flow conditions, which will be especially important when studying diffusion effects [178, 179]. The nanowire had a trapezoid cross-section with a close relation of the top width and the bottom width to the initial thickness of the Si layer. The aspect ratio is given by:

$$w_b = \frac{2t_{Si}}{\tan(57.4)} + w_t \qquad 4.1$$

with w_b is the width of the wire at the bottom, w_t is the top width of the wire and t_{Si} is the thickness of Si layer. With increased etching times the two planes (111) created a triangular cross-section of the SiNW. The surface roughness of the SiNWs after the

finished process was much smaller compared to the first process run (fig 4.4 (right)). In addition, the contact line was perfectly covered by the passivation layer as it can be seen in figure 4.4, left. This was due to the reduction of the hard mask oxide lead to decrease in step high between the contact line and the base plane after removing the mask oxide and also due to increase thickness of the passivation layer.

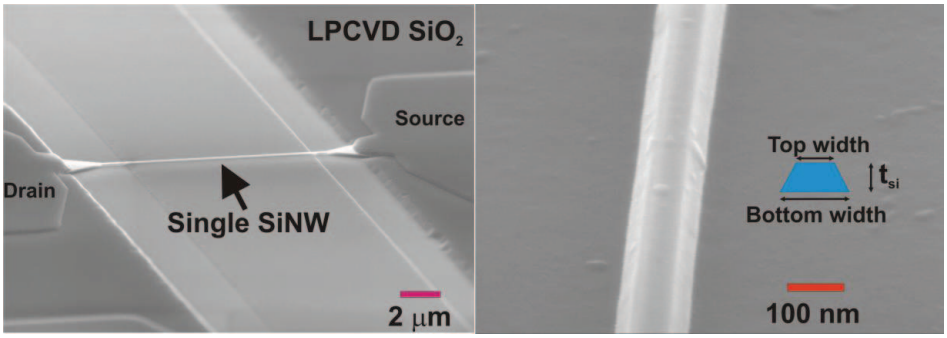

Figure 4.4. *SEM images of a single SiNW out of the second process run. It can be seen that the contact lines were perfectly covered by a good LPCVD passivation layer (left). The SEM image on the right shows a portion of a SiNW with a trapezoid cross-section having a very smooth surface (right).*

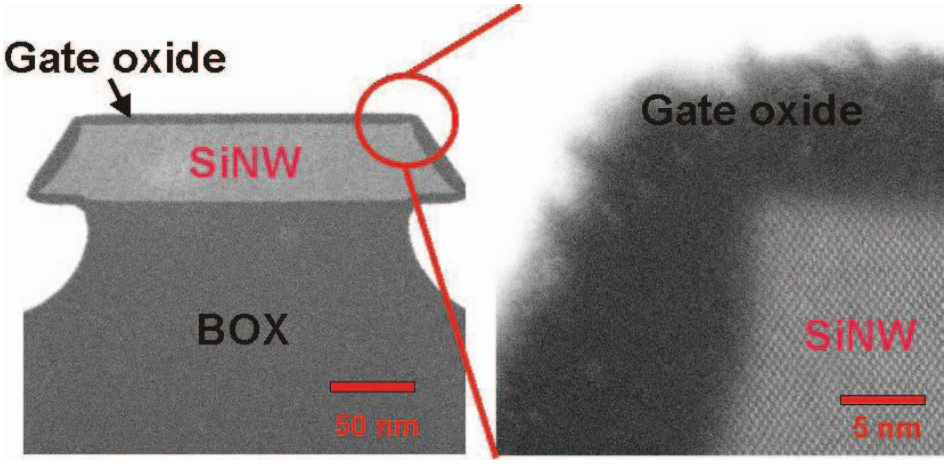

Figure 4.5. *A STEM image of the cross-section of a 360 nm (bottom width) SiNW prepared by FIB (left). The SiNW had a trapezoid cross-section. The undercut of the BOX layer was originating from the removal of the mask oxide layer after TMAH etching. This effect eventually leads to free standing small wires (less than 100 nm in this case). The gate oxide on the (111) plane was thicker than on the (100) plane as can be seen in the high resolution TEM image (right).*

To validate the final structure of the wires, cross section and the thickness of the gate oxide layer on the different plane of the SiNW structure, scanning transmission electron microscopy (STEM) analysis was used. In figure 4.5, the cross section of a 360 nm (bottom width) SiNW can be seen. The analysis revealed that the cross section was not an ideal trapezoid as it had quite spiky etches, especially at the bottom side of the wires. It can also be seen that the gate oxide grown on (111) was thicker compared to that on the (100) plane. Nevertheless, the whole structure was totally covered by the high quality oxide layer having a thickness of about 7 nm on the (100) planes and 13 nm on the (111) planes, respectively. The under etching of the BOX layer can be seen on the left and right side of the SiNW in figure. 4.5 (left). As discussed before, this was originating from several wet etching steps to remove the SiO_2 during fabrication processes. At an intersection of the (100) and (111) planes, figure 4.5 right, due to the competitive oxide growth at the intersection was not as sharp as the shape of the nanowire itself.

4.2. Electronic characterization of the SiNW arrays

The SiNW arrays were characterized by the back-gate and front-gate operation as shown in figure 3.7. The transfer and output characteristics of the SiNW as a function of voltages were carried out by using the measurement set up with the Keithley 4200 SCM system as shown in figure 3.8. Contact lines of the SiNWs were either kept at the same doping level as the original wafer (7×10^{14} ions/cm^3) or highly implanted by boron ions (1×10^{19} ions/cm^3).

4.2.1. Back-gate characteristics

a. SiNW chips without implanted contact lines

Typical back-gate transfer characteristics of SiNW without an ion implantation of the contact lines (*non-implanted contact lines*) is shown in figure 4.6. The back-gate voltage (V_{BG}) was applied to the silicon substrate as shown in figure 3.7 and swept from -30 V to 30 V in steps of 0.1 V. The transfer characteristics were recorded at different V_{DS}: 1.0 V (black curve), 2.0 V (red curve), and 3.0 V (green curve). There was no electrolyte solution on the front gate oxide in these measurements.

As can be seen in figure 4.6, the transfer characteristics of the SiNW correspond to three regimes: hold accumulation (a) at negative V_{BG} ($V_{BG} < V_{TH1}$), inversion or electron accumulation (c) at positive voltage ($V_{BG} > V_{TH2}$), and depletion or off-state at $V_{TH1} < V_{BG} < V_{TH2}$. Here V_{TH1} = -15 V is the threshold voltage of the hold accumulation regime and

V_{TH2} = 5 V is the threshold voltage of the inversion regime as shown in figure 4.6. Consequently, these SiNWs can be used as p-channel transistors (at negative V_{BG}) or as n-channel transistors (at positive V_{BG}).

Figure 4.7 presents a model to explain the above behavior of the devices with related energy band diagrams. In this process, there are two phenomena effective: First, the influence of the fixed charges at the oxide-silicon interface [180] and second, the Schottky barrier at drain contact and source contact between metal and low doped silicon [84, 181].

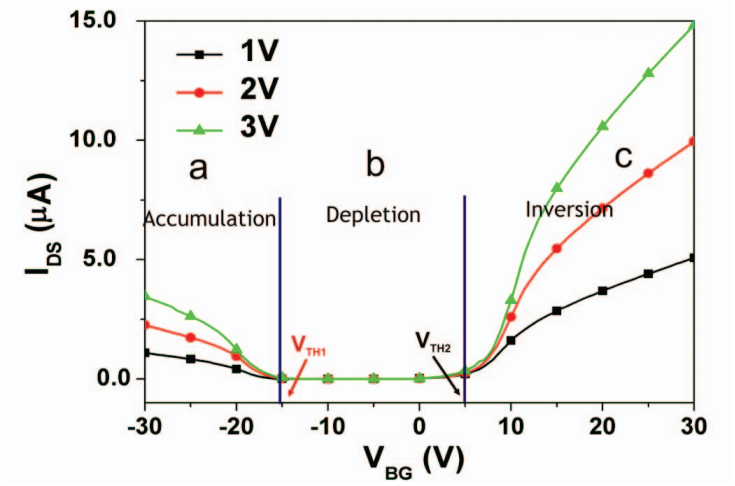

Figure 4.6. *Back-gate transfer characteristics of a SiNW transistor (380 nm × 3 μm). In this case, the drain-source contact lines have the same doping levels as the SiNWs. The transistors can be operated as p-type transistors or n-type transistors depending on the applied voltages to the gate.*

When the thickness of the Si layer becomes thinner (40÷60 nm), a depletion of free charge carriers occurs due to the fixed charge at the Si-SiO_2 interface [180]. Consequently, only the fixed charges close to the acceptor ions remain [157]. In this situation, there is no free charge in the channel and the transistor is in off-state (figure 4.7 b). When the back-gate voltage is sufficient, the free charges form in the channel. Consequently, the transistor is in on-state. Due to the same doping level of the contact lines and the nanowire, the energy state is constant on entire structures and there are only the different at the metal-silicon contact due to Schottky barrier [84, 181]. Depending on the bias condition of the back-gate voltage, the energy-band barrier of the silicon layer is bent and the bending directions are either up or down corresponding to electrons or holes formed in the channel. These carriers can tunnel through the barrier, thus, creating a current between source and drain [182]. For

a positive V_{BG}, the electron barrier is sufficiently low and the thickness of the barrier decreases, so that an inversion-electrons channel forms and turns on with electron conduction as major carriers (figure 4.7 c). On the other hand, an accumulation of the holes is formed for a negative V_{BG}, leading to a domination of the hole-carriers conduction (figure 4.7 a). Therefore the transfer-characteristic curves of this device shows 3 regions, accumulation of charges (hole carriers), depletion of charges (channel closed), and inversion of charges (electron carriers). Due to the lower effective mobility of hole compared to electron [84], the current amplitude of p-channel regime is smaller than the n-channel regime of the SiNW as can be seen in figure 4.6.

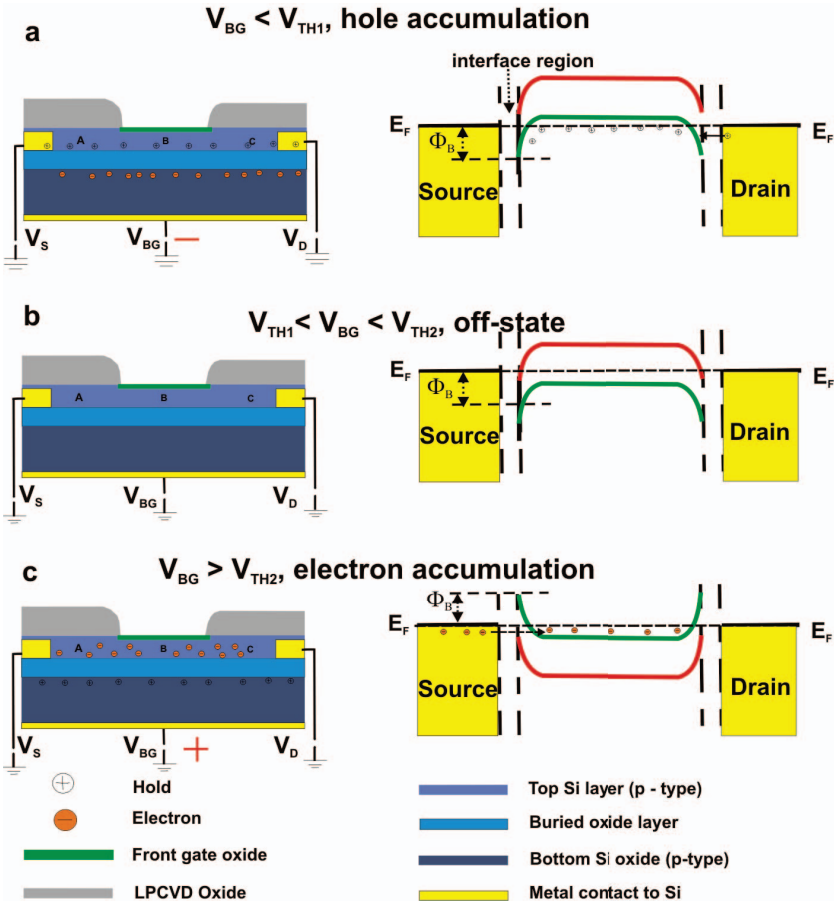

Figure 4.7. *Back-gate operation of the non-implanted contact line SiNW sensor without fixed front-gate potential. Depended on the back-gate bias, either holes or electrons can be formed in the channel, resulting in p-channel or n-channel transistor behavior, respectively.*

b. SiNW chips with a high boron implantation of the contact lines

The main part of our fabrication process relied on a high implantation of the contact lines. Due to the long and very thin Si contact lines in our chip designs, reduction in serials resistance in correspondence with a high implantation level of the contact lines was an important step to improve the performance of the devices. The consequences of a voltage drop across the contact lines or the effect of the serials resistance to the devices performance will be discussed later in this chapter.

The source and drain contact lines of the SiNW chips were implanted by Boron ions with a dose of 5×10^{14} ions/cm^2 that corresponds to a concentration of approximately 1×10^{19} ions/cm^3 for a silicon thickness of 50 nm. Detail about the implantation profiles on the chips was described in section 3.1.1. The resistances of the common source contact lines of both the 4×4 arrays and 28×2 arrays after ion implantation were in the range of 100 kOhm. These values are much lower compared to the non-implantation contact lines (about 1 MOhm) and do not strongly depend on the electric field (such as back gate voltage) as compared to the SiNWs without implantation contact lines. The metal-silicon contact was proven to be an *ohmic* contact.

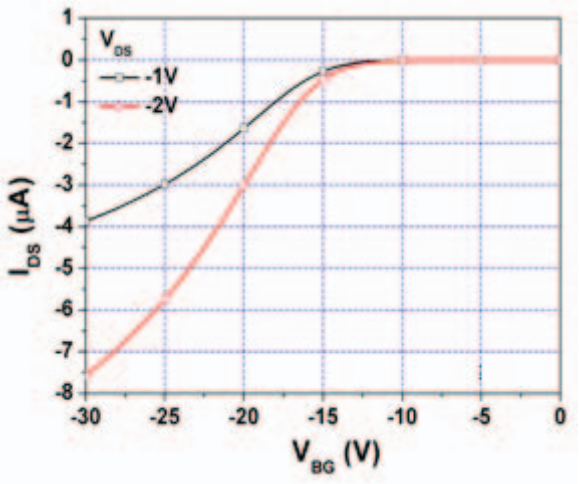

Figure 4.8. *Back-gate transfer characteristics of six parallel SiNWs (130 nm width and 3 μm length) transistors in air. The drain-source contact lines were highly doped with Boron ions (6×10^{14}ions/cm^2). The chips show a behavior like p-enhancement transistors with a threshold voltage of -13 V for the back-gate operation.*

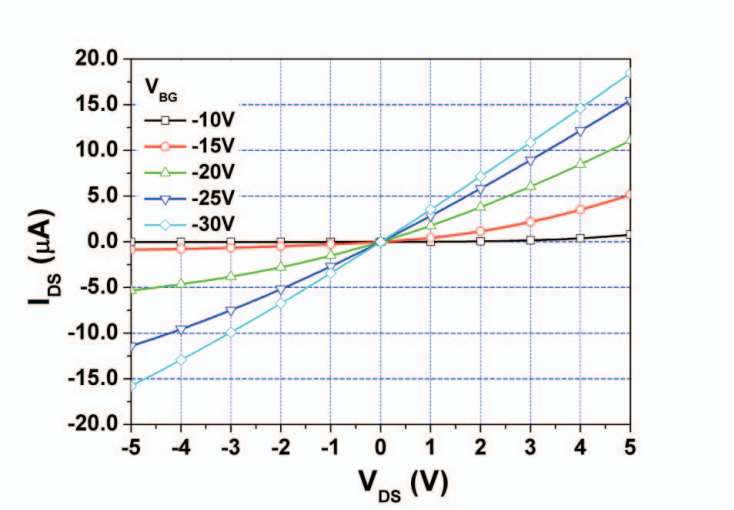

Figure 4.9. *Back-gate output characteristics of six parallel SiNWs (130 nm width and 3 μm length) in air. The drain-source contact lines were highly doped with Boron ions (6×10^{14} ions/cm^2).*

The electronic characterization of the devices with the back gate as gate voltage input was performed without electrolyte on the front gate side. The transfer characteristics were carried out by sweeping V_{BG} from -30 V to 30 V in steps of 0.1 V at a constant V_{DS} voltage. Figure 4.8 presents back-gate transfer characteristics of the implanted contact lines SiNWs out of 4×4 arrays, which contain six parallel wires (130 nm width and 3μm length). The I_{DS} (V_{BG}) characteristics of this device is plotted from -30 V to 0 V. Black curve represent for V_{DS} = - 1 V and red curve represent for V_{DS} = - 2 V, respectively. The output characteristics of the same device recorded by sweeping V_{DS} from -5 V to 5 V in steps of 0.1 V at different V_{BG} value from -10 V to -30 V in steps of 5 V (as shown in different colors) is presented in figure 4.9.

As can be seen in these figures, the devices exclusively showed an accumulation behavior of a typical p-channel enhancement transistor with a threshold voltage of -13 V. There is no n-channel transistor behavior in the whole range of V_{BG} from -30 V to 30 V (data not shown) as like the non-implanted contact line. The observed current of the device (I_{DS} = 4 μA at V_{DS} = -1 V, V_{BG} = -30 V) was much higher compared to the previous case of SiNW without implanted contact lines (1μA at V_{DS} = -1 V, V_{BG} = -30 V). The subthreshold slope for the structure was 1.3 V/decade. It was obviously, the implantation of the contact lines changed the behavior of the devices and enhanced the electrical performance compared to the non-implanted contact lines.

The output characteristics of the devices confirm that SiNW behave as a long-channel p-enhancement field-effect transistor. At V_{BG} = -10 V, the device operates in subthreshold region, consequently the current I_{DS} is not visible is the linear scale (black curve). When V_{BG} lower than V_{TH}, the output characteristics curves clearly show two regions: linear region (device act as a resistor) at $|V_{DS}| < |V_{GS}-V_{TH}|$ and saturation region at $|V_{DS}| > |V_{GS} - V_{TH}|$, respectively.

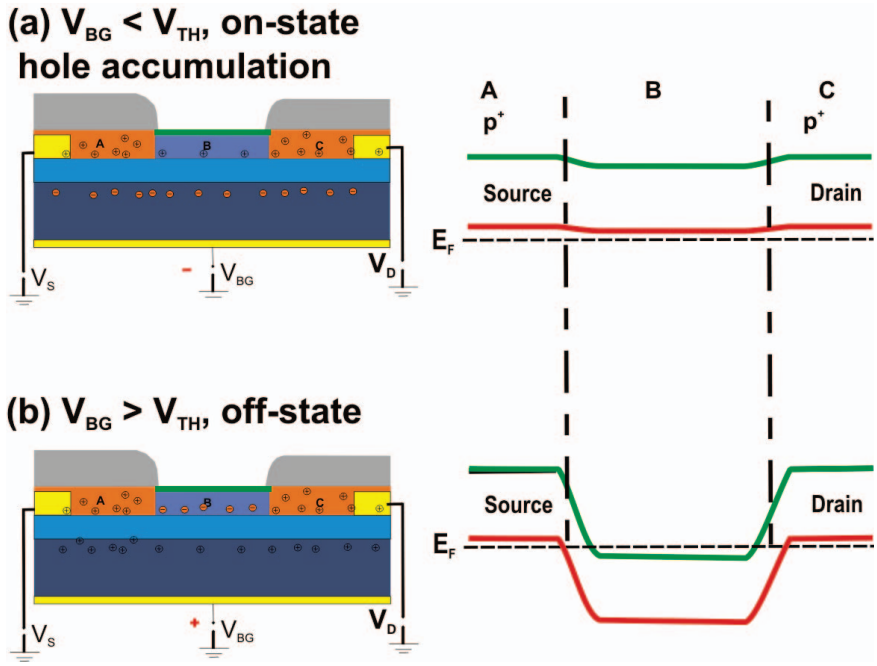

Figure 4.10. *Operation of a SiNW with high boron doped contact lines. At negative V_{BG}, an accumulation of hole is formed in the SiNW and the transistor is in the "on-state". At positive V_{BG}, an inversion layer of electrons is formed inside the SiNW. Due to the different polarization of the SiNW and contact lines, there is no current flow through the device. The transistor is in the "off-sate".*

A model to explain the operation mechanism of the devise is presented in figure 4.10. On the Si device layer, the high doping dose of source and drain contact lines are presented as regions A and C, respectively, while the low doping channel is presented as region B. The contact lines are degenerately doped semiconductor because of the high doping concentration of Boron ions used in our chip fabrication (10^{19} ions/cm^3). Within the applied V_{BG} in our experiments, the major carrier in the contact lines (A and C regions) are holes as shown in figure 4.10. As discussed above, due to the fixed charge at the Si/SiO_2

interface the region B is fully depleted of free charge carries [180]. A large negative bias voltage is needed to convert the region B into accumulation. When a sufficiently negative bias voltage applied to the gate ($V_{BG} < V_{TH}$), the energy barrier is reduced and the channel is holes accumulated as shown in figure 4.10 a, the NW is turned on as the p-enhancement mode FET. At positive bias V_{BG}, the energy barrier increases as shown in figure 4.10 b. An increase of V_{BG} to more positive lead to formation of an inversion layer of electron, however, due to the different polarity between contact lines and the channel there is no electric transport in the structure. The SiNW is off-state.

The transfer characteristics of transistors with different wire dimensions out of a 4×4 transistor array are shown in figure 4.11 in both linear scale and logarithmic scale. As it can be seen, the maximums of I_{DS} as well as the threshold voltages strongly depend on the width of the SiNWs. For small wires (80 nm and 130 nm width), the threshold voltages were approximately -13 V. In contrast, the threshold voltage of the 380 nm width one was determined to be -8 V and remained constant for all larger wires from 900 nm width to micro-scale wires (data not shown). However, in the curve of the large wire (380 nm and 900 nm), a small kink was visible at V_{BG} = -18 V. So far, the underlying reason for this kink could not be found. By extrapolating of the data of these curves from -30 V to -18 V, one can estimate that the intersection with the x-axis results to the same threshold voltage as for the small wires.

In the logarithmic scale, it can clearly be seen that the on-set of currents start at the same value of V_{BG} = -3.8 V for all the different wire widths but the small wires had much larger subthreshold slope compare to the large one. The values of the subthreshold slope were 850 mV/decade for the 380 nm and 900 nm wire widths, while it was 1.3 V/decade for the 130 nm wire width and 1.4 V/decade for the 80 nm wire width, respectively. There are two main mechanisms to explain this behavior:

- The first is the effect of the fixed surface charge. At the gate-oxide layer and in the Si-SiO_2 interface the fixed charges are always present caused by defects or unavoidable contaminations from the chip processing. The fixed charges are positive in this case and can block the conducting channel. In the smaller wires, the entire structure can be effected thank to the surface-to-volume ratio, and as a result the surface charge effect becomes more dominant compared to the larger one. Thus, the small wires need higher applied gate voltage to reach the flat-band voltage for holes [183, 184].

- The second is the effect of the undercut in the back-gate oxide layer underneath the nanowires. The under etching of the BOX layer during the fabrication process always was the same. Therefore, the area of the wires, which still is in contact with the BOX, was much less for wires with smaller widths. Therefore, the influence of the back gate is reduced for the smaller wire structures.

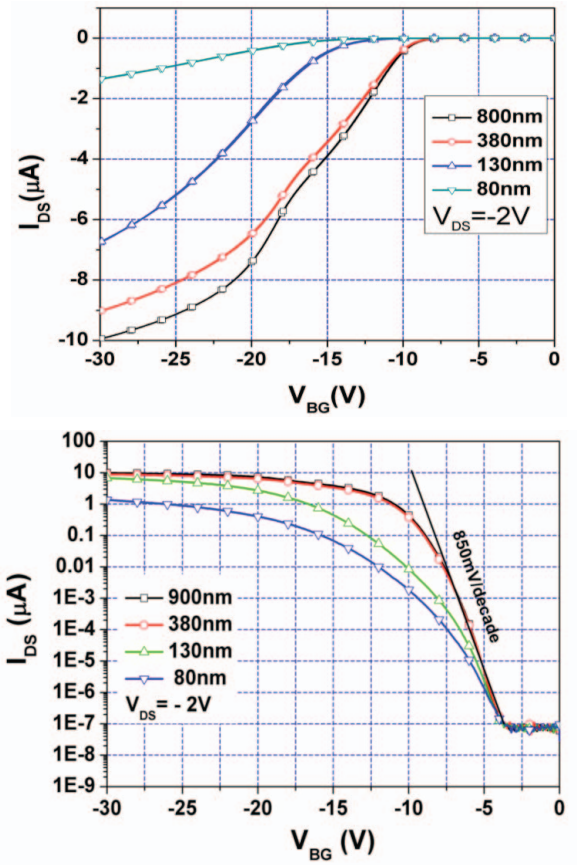

Figure 4.11. *Size effect of the back-gate transfer characteristics for the SiNWs with a high boron implantation of the contact lines. Each channel had six wires in parallel with the same length of 3 μm. The wires widths were 80nm, 130 nm, 380 nm, and 900 nm, respectively.*

4.2.2. Front-gate characteristics

The front-gate characterization was carried out as described in section 3.3. The front-gate voltage (V_{FG}) was applied through an electrochemical reference electrode immersed into the electrolyte solution was shown in figure 3.7. All the results shown in this section was

carried out with same condition (Titrisol buffer solution, pH 7, Merck). The back gate was keep floating during these measurements.

a. SiNW chips without implanted contact lines

Typical front-gate transfer characteristics of a SiNW without implanted contact lines are presented in figure 4.12. The chip had six SiNWs in parallel with a dimension of 130 nm × 3 μm in the 4×4 transistor arrays. The V_{FG} was swept from -2 V to 2 V and the V_{DS} were varied from 0 V to 3 V in steps of 0.5 V as shown in different colors of the curves. As can be seen, the devices shown only an n-channel transistors behavior with a threshold voltage of V_{TH} = 0.5 V. The same behavior was also observed with a larger variation of the front-gate voltage, from -3 V to 3 V. The p-channel transistor behavior like for the back-gate characteristics of these devices did not exist in the front-gate operation mode. This behavior is understandable, because the contact lines were passivated by a thick layer of LPCVD oxide, so that the low bias V_{FG} did not affect the charge carries of the contact lines. As discussed above, the fixed charges at the oxide interfaces can cause an inversion of electrons inside the Si layer [180]. This effect was clearer when the LPCVD oxide was employed as passivation layer due to the defect of the LPCVD oxide. Due to this reason, the charge carriers in the contact lines were always electrons, while the charge carriers in the SiNW structure can be fully controlled by the front gate voltage. Thus, a negative bias of V_{FG} creates an *npn* structure and an *nnn* structure for positive bias. In the *npn* structure with negative V_{FG}, there is no electric current flowing through the devices due to different polarization of the charge carriers between the contact lines and the SiNW. On the other hand, in the *nnn* structure the electric current can be controlled by the front-gate voltage V_{FG}. This effect is illustrated in figure 4.13.

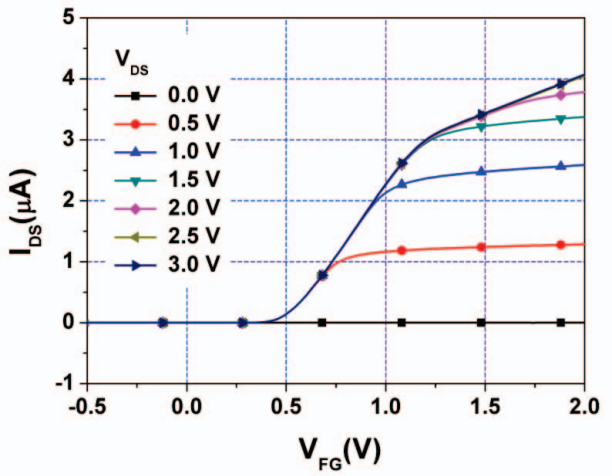

Figure 4.12. *Front-gate transfer characteristic of the non-implanted contact lines chip. The chip had 6 SiNWs in parallel and the width and the length of the wires was 130 nm and 3 μm, respectively. The chip showed an n-type transistor behavior over the range of V_{FG} from -2 V to 2 V (data for the V_{FG} from -2 V to -0.5 V are not shown).*

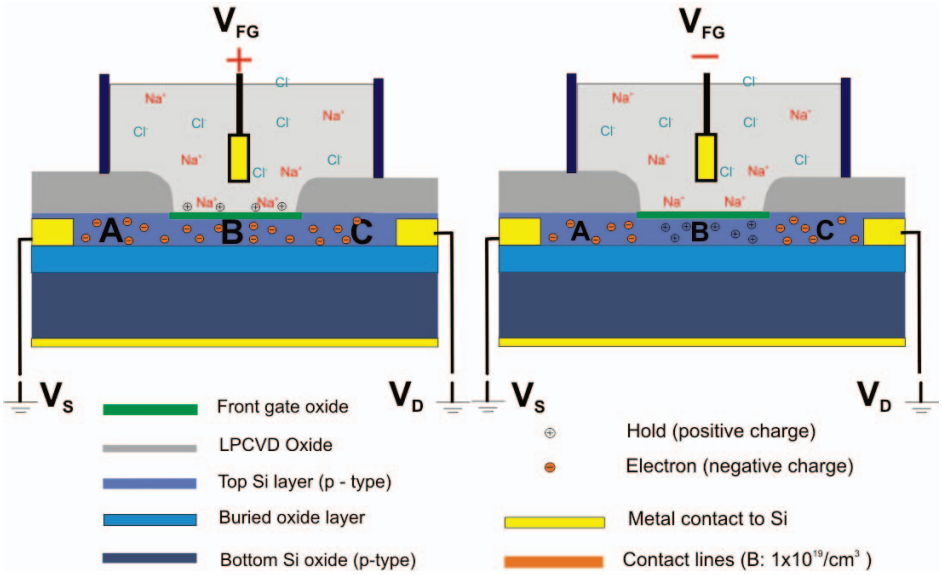

Figure 4.13. *Front-gate operation principle for the SiNWs with non-implanted contact line.*

As can also be seen in figure 4.12 the transfer characteristics curves are overlap at V_{DS} > 2.5 V, yellow and dark blue curves. The current I_{DS} did not increase further at V_{DS} higher than that value. It means that the largest I_{DS} of the devices were achieved at a maximum of V_{DS} = 2.5 V. The current I_{DS} were saturated even if the V_{FG} was increased. This effect was caused by the high source and drain resistances and the contribution of the Schottky barrier at the metal-silicon interface as discussed above in section 4.2.1.a.

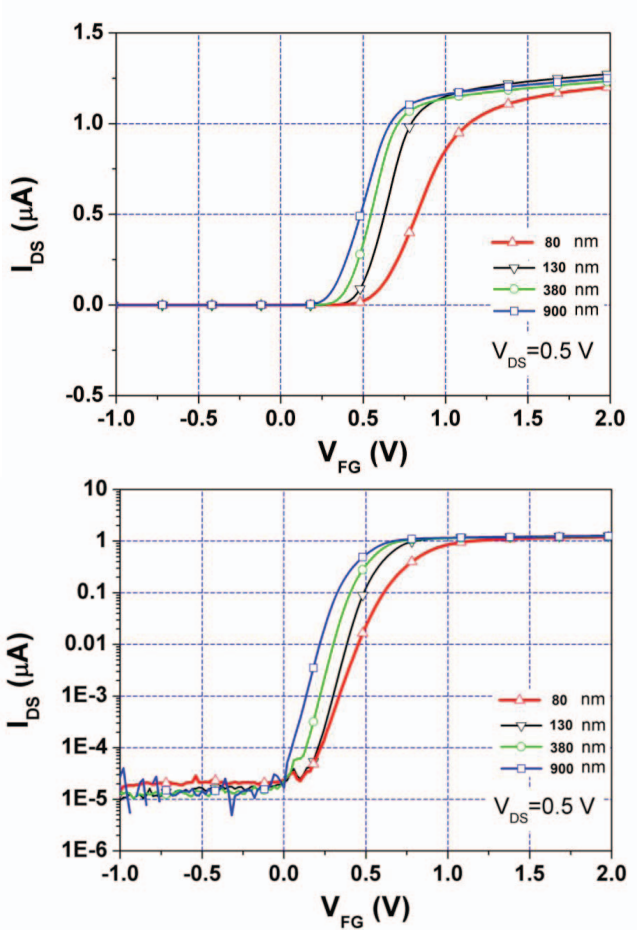

Figure 4.14. *Front-gate transfer characteristic of SiNWs with non-implanted contact lines with different geometry of the SiNWs. The length of the wires was 3 μm in all case. The data are shown in linear scale (left) and logarithmic scale (right) for V_{DS} = 0.5 V*

The threshold voltages of SiNW devices also depended on the size of the wires. The smaller wire widths had higher threshold voltages compared to large ones. A comparison

of the transfer characteristics of the different wire widths is presented in figure 4.14 in both linear and logarithmic scales. It can clearly be seen that the threshold voltages increase with decreasing wire diameters. Subthreshold slope extracted from figure 4.14 were determined at approximately 90 mV/decade for the 130 nm, 380 nm and 900 nm wire widths and 100 mV/decade for 80 nm wire width.

b. SiNW chips with a high boron implantation of the contact lines

6 parallel wires on 4x4 arrays out of first fabrication process

Figure 4.15 shows the transfer characteristic of the 6 SiNWs (130 nm ×3 µm) out of the 4×4 arrays of the first fabrication process in linear scale and logarithmic scale. The V_{FG} voltage was swept from 0 V to -3 V and the V_{DS} voltage was varied from 0.0 V to -2.0 V in steps of -0.5 V. The SiNWs presented p-channel enhancement transistors and had the V_{TH} of about -0.7 V. The subthreshold slope extracted from the transfer-characteristic curve in the logarithmic scale is 90 mV/decade. As discussed above, the p-channel enhancement mode of the devices is a result of the depleted charge carriers in the SiNW due to fixed charges at the oxide layers [84, 180, 181].

Figure 4.16 shows the output characteristics of the SiNW chips with a wire width of 130 nm and a length of 3 µm. The V_{DS} voltage was swept from -3 V to 3 V and the V_{FG} voltage was applied from 0.0 V to -3.0 V in steps of -0.5 V. At V_{FG} = 0.0 V, which is below the threshold voltage, there is no electric current flow present between source to drain as related to the value shown in the logarithmic scale in figure 4.15. When $V_{FG} > V_{TH}$, I_{DS} increases and shows a linear behavior at low V_{DS} due to $I_{DS} \sim (V_{GS} - V_{TH})V_{DS}$, and a saturation at high V_{DS} due to $I_{DS} \sim (V_{GS} - V_{TH})^2$. In this situation, the SiNW transistors behave like long-channel field-effect transistors as described in section 2.1.

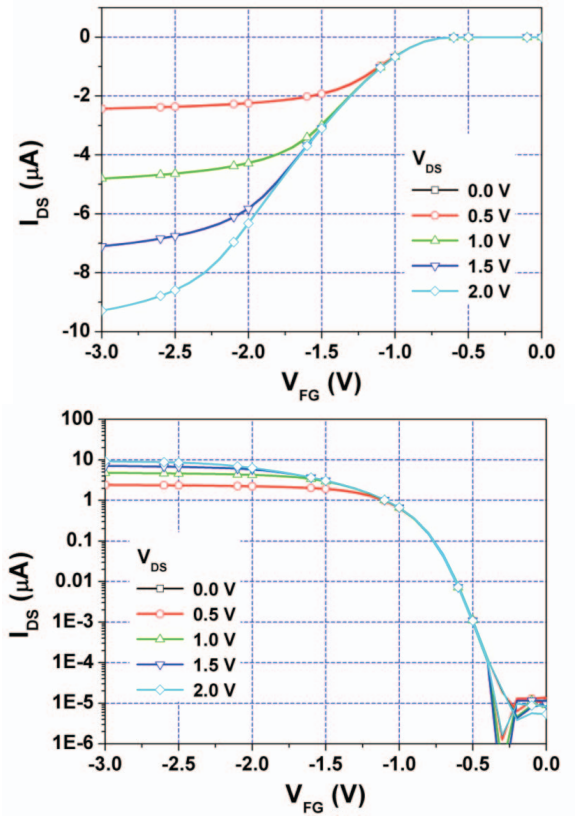

Figure 4.15. *Typical front-gate characterisitics of SiNW with high boron doped contact lines. The chips show a p-enhancement transistor behavior with a threshold voltage of -0.7 V.*

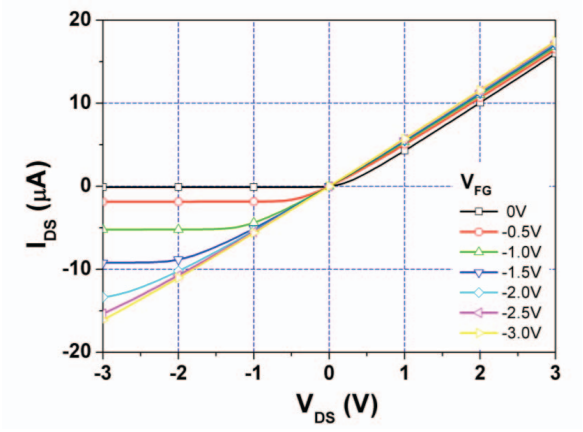

Figure 4.16. *Output characteristic of a 130 nm × 3 μm SiNW on 4×4 arrays (6 NWs in parallel)*

The transfer characteristics of the SiNWs out of the 4×4 transistor arrays of the first process with different width are shown in figure 4.17. It can clearly be seen that the smaller wires have a higher threshold voltages and a larger subthreshold slope. This behavior is similar to the performance of the chip with non-implanted contact lines. As discussed previously, this behavior is caused by influence of the interface charges. Another effect is that in general the front-gate oxide is thicker in average when the diameter of the wires is smaller. The reason for this is that for smaller wire the (111) plane is dominating and in general the gate oxide growth is faster at the (111) plane as discussed in section 4.1. As it can be seen in figure 4.5, the gate oxide layer is thicker on the (111) plane. This leads to an increase of the threshold voltage due to equation 2.1. Here, the threshold voltage is a function of the gate-oxide capacitance. It is also noted that the interface charges are dominating inside the smaller wire structures. In this case, the smaller wires need a higher gate voltage to reach the flat-band voltage. The same explanations as already described in section 4.2.1 for the back-gate characteristics are also applying for the front-gate characteristics.

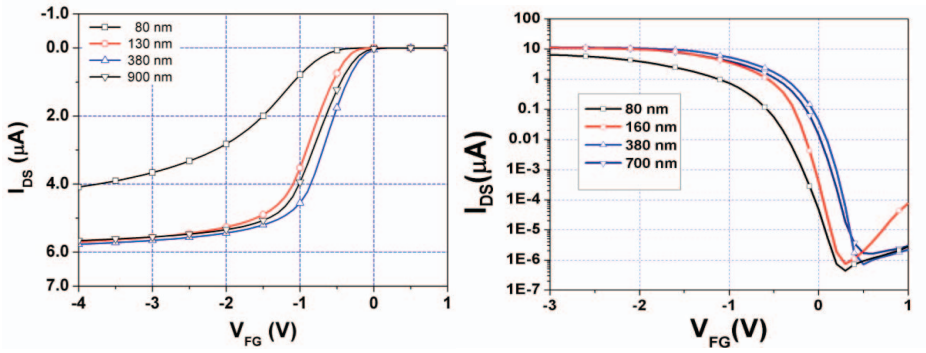

***Figure 4.17**. Front-gate characteristic of the SiNW chips with different wire diameters.*

Single wire on 28x2 arrays out of second fabrication process

In the second fabrication process, the chips were design differently compared to the first fabrication process. In this design, one sensing point had a single SiNW, which was addressable between comment source and individual drain contacts. To eliminate the effect of the serials resistance that will be discussed later, the drain source contact lines were implanted with higher dose of Boron ions. As shown in section 3.1.1, the wire lengths were 5 µm, 10 µm, 20 µm and 40 µm and the wire widths were 200 nm and 400 nm in the mask design. The SiO_2 gate oxide was about 7 nm on (100) plan as shown in figure 4.5.

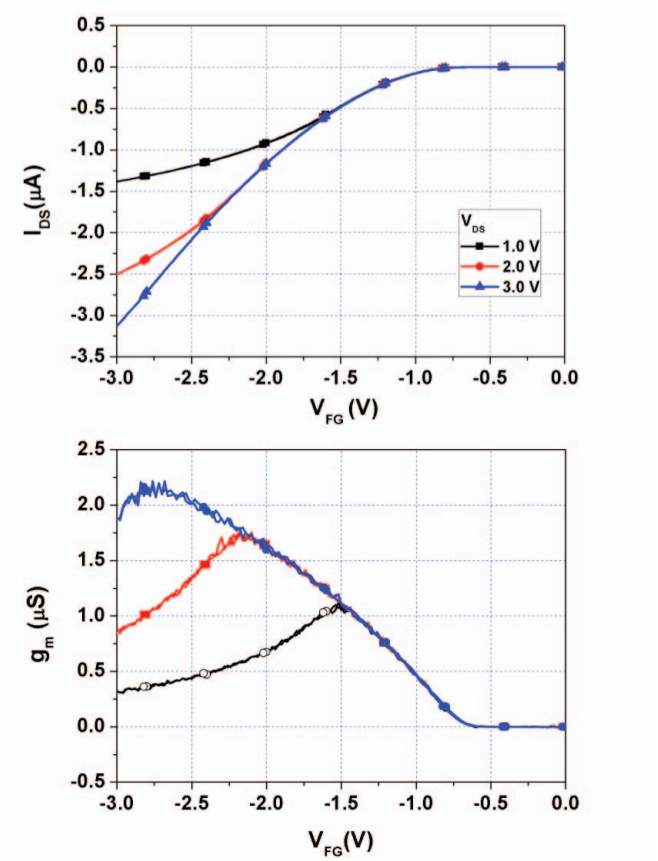

Figure 4.18. *Front-gate transfer characteristics of a single SiNW out of the second fabrication process. The wire had a width of 160 nm and a length of 10 μm.*

Typical transfer characteristics and output characteristics of the single SiNW out of the second generation chips are shown in figure 4.18 and figure 4.19, respectively. The SiNW had wire width of 160 nm and wire length of 10 μm. The devices shows p-channel transistor behavior and a long channel effect with a threshold voltage of – 0.7 V as expected from the above results. The devices show better performance compared to the first chip design. Due to small and long wire, the resistance of the SiNW was dominating in the working condition as can be seen from the transfer characteristics of the devices. The current amplitude of the devices is much smaller compared to the first generation of 4×4 arrays. Depending on the wire dimension, the I_{DS} were in the range from 300 nA to 3 μA so that the maximal transconductance were also varied from few hundred nS to around 2 μS in the working voltages. The long wires showed smaller current than the short one

because their resistances were scaling in correspondence with the wire lengths. The mobility of holes was calculated for the devices are about 100 $cm^2/(Vs^{-1})$.

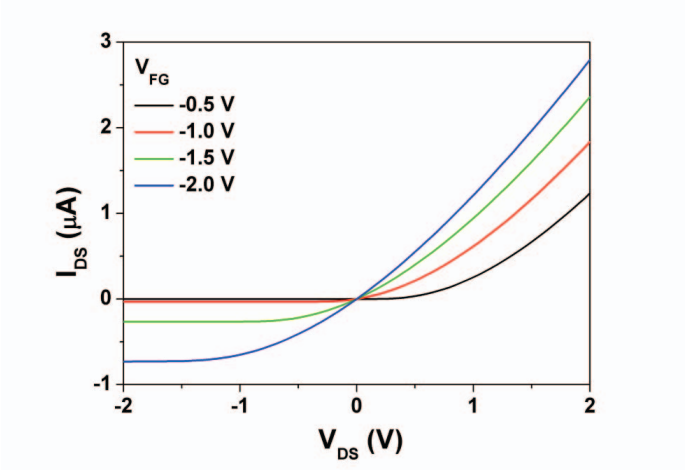

Figure 4.19. *Output characteristics of a single SiNW out of the second fabrication process. The wire had a width of 160 nm and a length of 10 μm*

A comparison of the different wire geometry is shown in figure 4.20. The subthreshold slope achieves 85 mV/decade for the short wires (less than 10 μm lengths) and increases when the length of the wire increases. This effect can be explained by an increasing charge scattering in a smaller and longer wire.

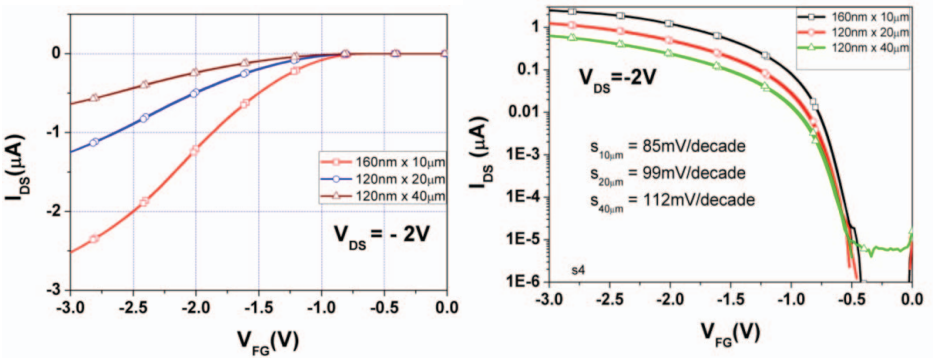

Figure 4.20. *Transfer characteristics of different wire geometry in linear scale and in logarithmic scale.*

A comparison of SiNW having the same length but different width is shown in figure 4.21. The threshold voltage dependence with respect to the size of the SiNWs is barely visible. This is a direct result of the changes in the chip fabrication protocol, which reduced the interface charges of the gate oxide compared to the first fabrication process.

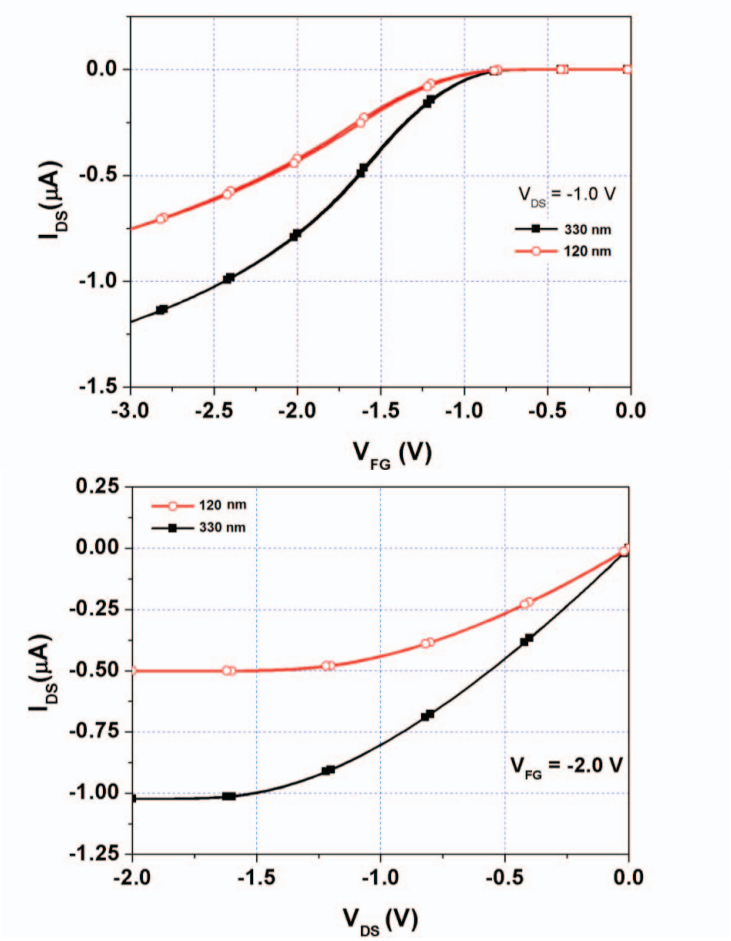

Figure 4.21. *Output and transfer characteristic of a SiNW chip with individually addressable wires. The wires have a length of 20 μm and a width of 120 nm (red curve) or 330 nm (black curve), respectively.*

4.2.3. Influence of the contact lines resistance effect to the SiNW arrays characteristics

The influence of the contact lines resistance is an important aspect for the performance and the reliability of the devices. The contact line resistances are generally very high due to the thin and long contact lines. In designs, the source contact line and the drain contact line resistances are about 100-150 kOhm and about 150 kOhm, respectively, leading to a total contribution of the serial resistance of 300 kOhm. The resistance of the SiNW structure alone depends on the applied V_{FG}, while the resistances of the contact lines are

independent of the applied V_{FG}. At high V_{FG}, the resistance of the SiNW decreases and the resistance of the contact line dominate. This effect can be seen in the change of the shape of the transfer-characteristic curves (figure 4.14). As a result the I_{DS} saturates at high V_{FG} caused by the contribution of the contact line resistance. In the transfer characteristics of the 4×4 array with six nanowires in parallel, the I_{DS} saturate early with increasing V_{FG}. At a certain value of applied voltages (V_{FG} and V_{DS}), the resistance of the contact lines dominates, which leads to a change in the transfer-characteristics curves.

To explain the influence of the contact line resistance, the equation 2.8 and 2.9 need to be extended by *ohmic* contact resistances R_S and R_D in serial at source and drain contacts. Which a certain V_{FG} and V_{DS} applied voltage, the respective effective voltage (V_{eff}) are:

$$V_{FG,\,eff} = V_{FG} - I_{DS}R_S \qquad 4.2$$

and

$$V_{DS,\,eff} = V_{DS} - (R_S - R_D)I_{DS} \qquad 4.3$$

By replacing the equation 4.2 and 4.3 to the equation 2.8and 2.9, the I_{DS} of the p-type channel transistor is given by

$$I_{DS} = \mu_p C_{ox} \frac{W}{L}\left([V_{GS} - R_S I_{DS}] - V_{TH} - \frac{V_{DS}-(R_S-R_D)I_{DS}}{2}\right) \times \\ \times\ (V_{DS} - (R_S - R_D)I_{DS}) \qquad 4.4$$

for the linear region and

$$I_{DS} = \mu_p C_{ox} \frac{W}{L}(V_{GS} - R_S I_{DS} - V_{TH})^2 \qquad 4.5$$

for the saturation region.

In these two equations, R_S and R_D are the resistances of the source and drain contact, respectively.

At low I_{DS}, the small correction factor $R_S I_{DS}$ to the large gate-voltage term (V_{GS}-V_{TH}) can be neglected, and only the total resistance matters. While at high I_{DS}, the term $R_S I_{DS}$ needs to be taken into account.

The serial resistances of the contact lines also affect the reliability of the large array. Inside the large array, the SiNWs are located in different places with different source-and drain-contact lengths. This affects the performance of the array device. Usually in our chip design, only one working point was set for the entire chip. Therefore the source bar resistance also limits the performances, when all channels of the large array are operated at the same time. In this case, the respective current I_{DS} for each wire will be limited by the respective source resistance.

For the 4×4 array of the first design, the influence of the serial resistance of the contact line dominates due to the parallel operation of six nanowires at one gate contact, as it was already described in detail by Eschermann [185]. By using a mathematic correction factor the influence of the serial resistances can be eliminated.

In the second design, the influence of the serial resistances was eliminated technically by increasing the resistance of the nanowires and elevating the doping level of the contact lines. In addition, the longer wires are advantageous for sensing applications and are also improving the performance of the arrays.

Figure 4.22 show the transfer characteristics of different channels out of the 28×2 arrays. The graph shows that the electric behavior is identical for all channels irrespective of their position in the array. In comparison to the 4×4 arrays of the first design, the difference of the current I_{DS} is negligible.

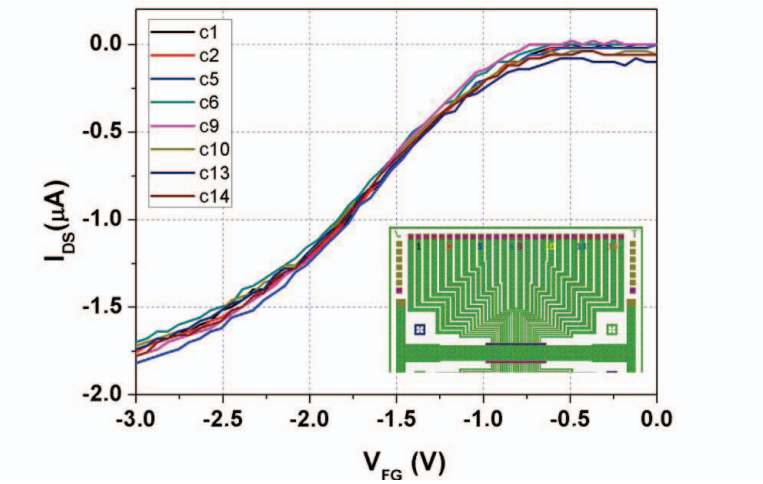

Figure 4.22. *Front-gate characteristics of different channels out of a single SiNW design (160 nm × 10 µm) of the 28×2 arrays. Compared to the first design, the influence of the contact line resistance was eliminated due to the high resistance of the SiNWs.*

4.2.4. Coupling of back-and front-gate

One of the specific properties of SOI-based devices, in general, or our SiNW in particular is an electrostatic coupling of the back-gate and front-gate contacts. This means that the back gate bias can be influenced by the front gate bias or vice versa. In most publications, the back-gate voltage is used to operate the SiNWs for biomolecular sensing, without controlling the potential of the front-gate electrolyte. That is a critical point, since the front

gate has a large influence in the electrochemical sensing experiments. If the potential of the electrolyte was kept floating, this was always leading to an instability of the signal [73, 75]. As discussed above, the back-gate operation of the device was not stable at all, especially when the electrolytes solution on the front-gate side of the SiNWs was exchanged. This leads to a systematic error for biochemical sensing, that mostly occurs at the front oxide.

The relation between the back-gate and the front-gate contact for fully depleted or partly depleted SOI-based electronic devices was already discussed in detail in text books [156, 157].

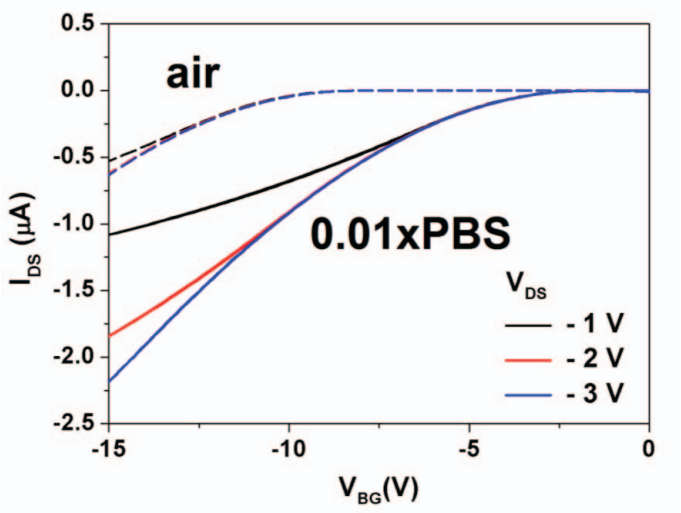

Figure 4.23. *Back-gate transfer characteristic of a SiNW chip with front oxide in contact to air (dashed lines) or to an electrolyte solution (solid lines).*

Figure 4.23 shows the transfer characteristic of a single 120 nm × 20 µm SiNW before and after the electrolyte was introduced to the front gate side. The electrolyte was not kept at a fixed potential, e.g. by a reference electrode. It can be seen that the back-gate characteristics of the SiNW changes strongly after the introduction of the electrolyte solution to the front-gate side. In particular, the threshold voltage shifted from -10 V to -2.5 V and the current amplitude was strongly increased. This effect was consistent for all the measurements with a first time introduction of the electrolyte solution.

When the electrolyte solution was introduced, *amphoretic* groups are forming in the front–gate side. These groups create a negatively charge at the front-gate oxide–electrolyte interface as described in section 2.2. The surface charges at the front gate can accumulate the holes inside the transistor channel.

One of the disadvantages of these devices is the reliability of their performance, which needs to be improved. A fluctuation of the threshold voltage has been observed when the electrolyte solution was exchanged. Each time, a new portion of the buffer solution was exchanged; a change in the threshold voltage was detected. Big shifts of the transfer characteristic to the left or to the right in comparison to the previous recording were observed. In other cases, no changes could be detected at all. To further investigate this instability, the unstable surface charges at the front oxide need to be taken into account, if the back-gate operation should be used for sensing. Without a controlled potential of the electrolyte solution, any disturbance of the system may change the charges at the oxide–electrolyte interface leading to instability of the threshold voltage.

The influence of the back-gate voltage to the front-gate transfer characteristics of single SiNWs out of the second design (330 nm width and 10 µm) is shown in figure 4.24. The back gate was biased at V_{BG} = -30 V (blue curve), V_{BG} = 0 V (black curve), and V_{BG} = 30 V (red curve), respectively. At V_{BG} = -30 V, the hole carriers accumulate in the SiNW leading to a decrease of the front-gate threshold voltage compared to the threshold voltage at V_{BG} = 0 V. This effect was unexpected, because at this voltage the device should work in accumulation mode as shown before in figure 4.8. When V_{BG} = 30 V, the front-gate threshold did not change, however, the current amplitude was smaller compared to V_{BG} = 0 V.

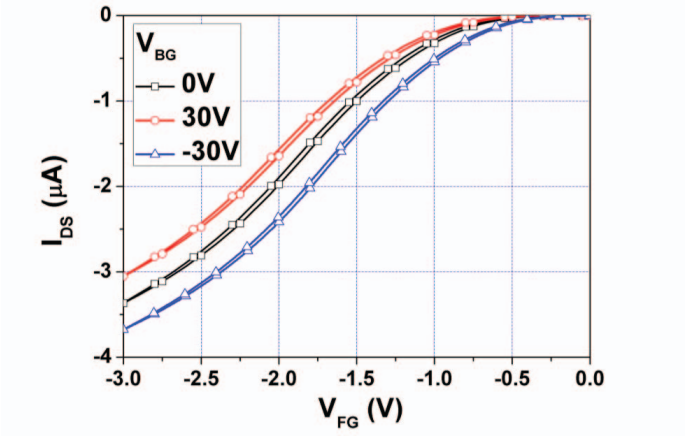

Figure 4.24. *Transfer characteristic of the front-gate voltage with different back-gate voltage.*

In the experiments in this thesis, the front gate was always dominating the conductance of the wires. If the front-gate voltage was applied at any potential, the effect of the back-gate

voltage was somehow eliminated. The current behavior was dependent on the front-gate voltage and only slightly changed with changing back-gate voltage. The effect of the front-gate voltage to the back-gate transfer characteristics is shown in figure 4.25 for two different wire widths: 130 nm on top and 300 nm at the bottom, respectively. It can be seen from the cross section of the wire shown in figure 4.5, that the small wire was nearly free-standing, so that the front gate nearly became a wrapped–all–around gate of the wire. Therefore it shows a stronger electrostatic coupling to V_{FG} compared to the wider wire. For the larger wire (300 nm width, bottom figure) the influence of the back-gate voltage is stronger because of the larger contact area of the BOX to the SiNW. This effect needs to be taken into account, when using the wires for biosensing as well as for future chips designs and fabrication processes.

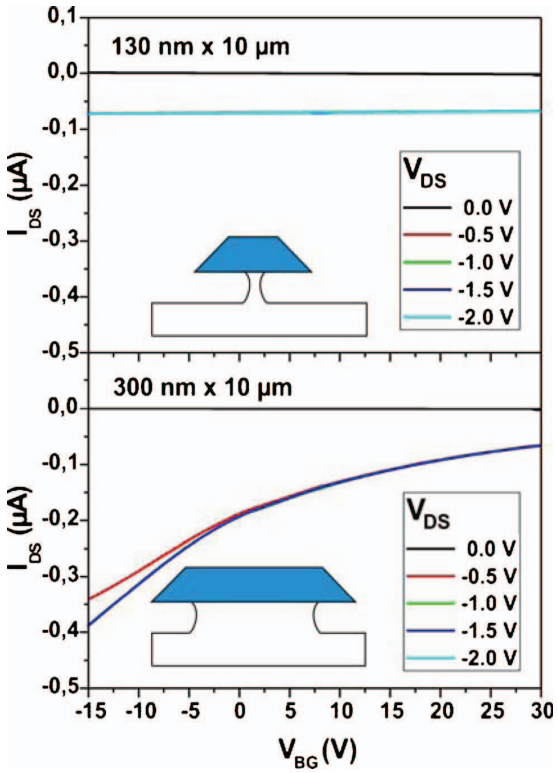

Figure 4.25. *Back-gate transfer characteristics of the SiNW of different width as indicated by the schematic cross-section at V_{FG} = -1.0 V.*

4.2.5. Signal reliability

Electric signal reliability of the SiNWs is an important factor for all sensing applications. The more stable the electric signals are, the less errors can be introduced by side effects.

Hysteresis

Generally, the transfer characteristics of the SiNW transistors showed a hysteresis behavior, when the gate voltage was swept forward and backward. The front-gate characteristics showed a small hysteresis while the back-gate characteristics showed large hysteresis. In addition, the hysteresis effect was dependent on the scan rate during recording. The underlying reason for this behavior could be the presence of fixed surface charges at the gate oxide, which seem to be polarizable. The hysteresis of the chip with different scan rates for the back-gate voltage to the transfer characteristics curve with the front oxide in contact to air is shown in figure 4.26.

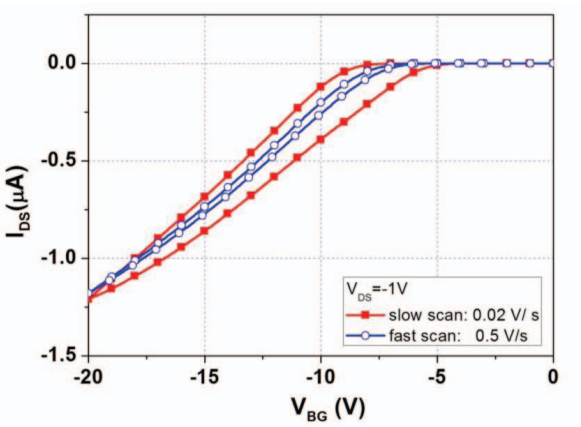

Figure 4.26. *The hysteresis effect of the back- gate transfer characteristics of the SiNW chip, which become visible with different scan rates.*

Drift

Signal drift is a well-known behavior of field-effect devices in electrolyte solutions, especially when SiO_2 is used as gate oxide [186, 187]. The drift behavior of the front-gate transfer characteristics of the SiNWs was really small and mostly was not visible if transfer-characteristics curves for different measurements at the same condition were recorded. However, the long term drift of I_{DS} after a working point was set is a coherent problem of FET devices, especially when the devices are operated in side an electrolyte solution. Figure 4.27 shows the drift of the signal over time for the *in situ* measurement. The current I_{DS} decrease very fast in the first 500 seconds and nearly saturated afterwards. The ΔI_{DS} was about 1.5% of the total I_{DS} and did not depend on the working point. However, this effect needs to be taken into account for all the in situ measurement.

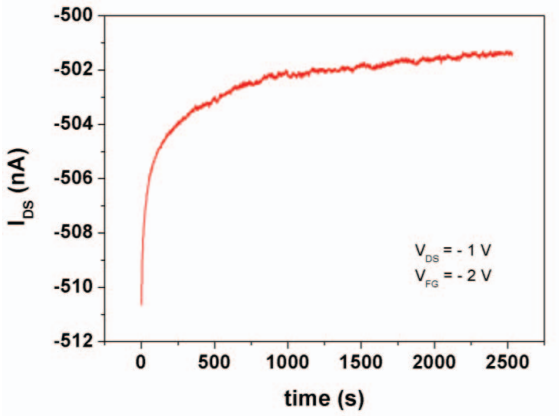

Figure 4.27. *Drift of the current I_{DS} versus time after a working point was set.*

Effect of plasma cleaning to the SiNW characteristics

For biosensor applications, the oxide surface needs to be functionalized with specific catcher molecules that bind reliably to the probe molecules. The quality of the functionalization process such as silanization also depends on the initial treatment of the SiO_2 surface. For the SiO_2 surfaces, either amino silane (APTES) or epoxy silane (GPTES) was used to create a covalently bound, bio-functionalized surface. In most publications, the surfaces are treated with oxygen plasma for cleaning of organic contaminations and activation of SiOH groups for a good coverage of the silane molecules on the surface. However, the oxygen plasma also affects the electrical properties of the nano-electronic devices. Figure 4.28 show the transfer characteristics of the SiNW chip before and after surface treatment with oxygen plasma with the parameters given in table 4.4. Obviously, the oxygen plasma degraded the electric performance of the SiNWs devices by inducing surface charges at the oxide surface. In our experiments this change was found to be irreversible. Further use of oxygen plasma leads to even a higher degradation of the devices. We performed many trials with different parameters of the oxygen plasma, but none of them gave sufficient results. Therefore, oxygen plasma was not further used as cleaning and activation procedure in this thesis.

Gas	Pressure	Power	Time
O_2	0.6 mbar	~10 W	2 min

Table 4.4. *Parameters for cleaning and activation of the oxide surface of the SiNWs prior to the silanization process. The process was carried out using a low pressure plasma system (Pico, Diener electronic GmBH, Germany).*

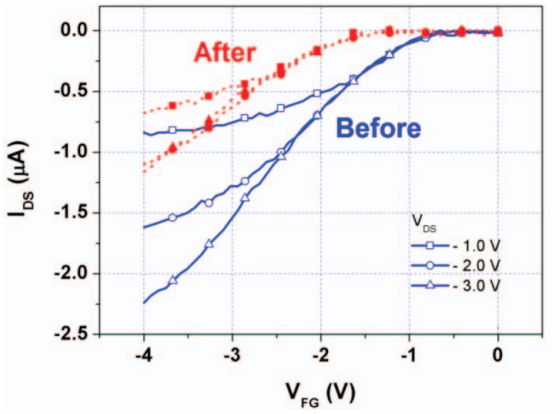

Figure 4.28. *Front-gate transfer characteristic of the SiNW before (blue curves) and after (red curves) oxygen plasma treatment.*

4.2.6. Transfer functions of the SiNWs.

Figure 4.29 shows the transfer function of the SiNW chips measured with the custom-made amplifier measurement set up (figure 3.13). A small sinusoid signal (10 mV) was applied to the reference electrode with the frequency ranging from 1 Hz to 1 MHz. The transfer functions of the SiNWs behave similar to the transfer functions of the micro scale ISFET of our group [42, 188]. Mainly the chips together with the first amplifier stage formed a low pas filter. The distortion of the transfer function curves at higher frequencies (above 10 kHz) was caused by the electronic hardware of the amplifier.

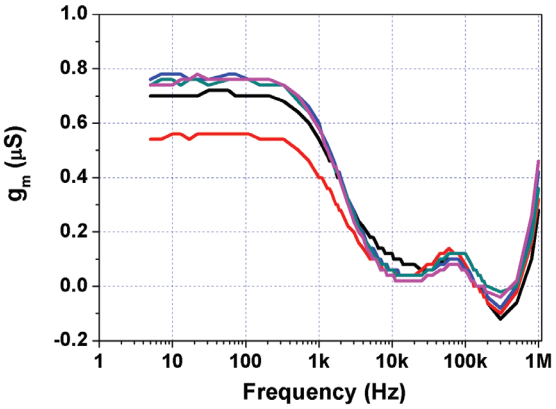

Figure 4.29. *Transfer function of a 160 nm × 10 µm SiNW in 0.01× PBS buffer, (pH 7)*

Figure 4.30 shows the transfer function of the SiNWs, which were measured in different NaCl solution from 0.01 mM to 10 mM. H(ω) represents the normalized value of the transconductance g_m. The increase in the cut-off frequency with increasing NaCl

concentrations is mainly caused by the change of the electrolyte conductivity. The underlying principles of this effect were already described in section 2.2. This effect was previously employed to observe the electrolyte conductivity [42, 111, 158].

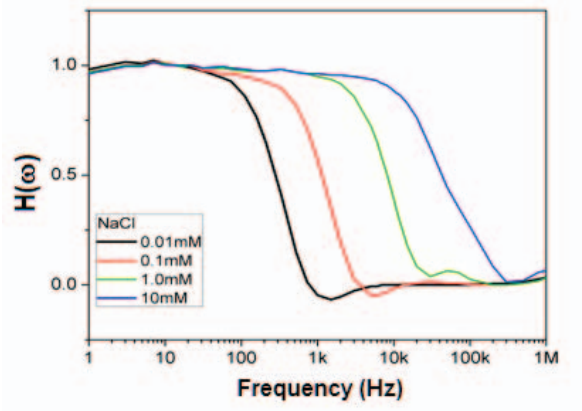

Figure 4.30. *Transfer function of one channel output composed of 6 SiNWs (130 nm × 3 µm) in parallel of the 4×4 array chips with different concentration of the electrolyte solution.*

4.3. Summary and discussion

The SiNW sensors were successfully fabricated and characterized. In the chip fabrication process, novel methods were applied by using a nanoimprint lithography technique in combination with anisotropic etching of silicon using TMAH. The process is a high throughput compatible and a mass production would be possible.

Nanoimprint lithography is a novel and powerful tool to fabricated nanostructures. However, the combination of nanoscale and microscale structures in one step of thermal imprint lithography is a big challenging due to the *proximity effect* as discussed in section 2.3. By a modified treatment of the residual resist layer and by a change of the layout design, the *proximity effect* of our thermal imprint process was minimized. In the second design with the 28×2 arrays, the residual resist layer was evenly distributed over the large area of the chips as well as over the whole 4 inch wafer. As a result, the fabrication process is reliable with a very high yield of devices on wafer (more than 90%).

By using TMAH anisotropic etching of Si on SOI wafer with defined SiO_2 nanostructures as a hard mask, the SiNW had a trapezoid cross-section with a very smooth surface. The size of the SiNWs can be tuned by controlling the etching time. The variation of wire widths were about 10 nm for the same design on the wafers and mostly cause by the mold

fabrication. A 60 nm bottom width of the SiNWs was achieved with the length of the wire up to 40 μm.

A very smooth surface of the finished SiNWs was achieved in the second process compared to the first process. Reason for this improvement was the thin oxide layer, which was grown on the Si layer before deposition of the LPCVD oxide. As a result, the SiNW arrays of the second process had high quality and a stable functionalization was possible. The electronic signals were stable in the electrolyte environment, because of the high quality LPCVD oxide layer passivation of the contact lines. The electronic characterization of the SiNWs were carried out thoroughly with both designs (4×4 array of the first generation and 28×2 array of the second generation) using either back-gate or front-gate operation. The properties of the SiNW are summarized in table 4.5. The non-implanted contact line chips showed both p-channel and n-channel transistors behavior with back-gate operation, while the SiNWs with highly boron doped contact lines showed only a p-channel transistor behavior. The back-gate operation with electrolyte on the front-gate side without any control of the front-gate potential was very instable in all experiment and could not be used for sensing applications.

The front-gate characteristics showed that the SiNWs with non-implanted contact lines were n-channel transistors and the SiNWs with highly boron doped contact lines were p-channel, enhancement-mode transistors. Generally, in contrast to back-gate operation, the electric signals of the front-gate operations were stable and reliable. A subthreshold slope of 90 mV/decade indicated that a high quality front-gate oxide was achieved in our fabrication process, which can enhance the sensitivity of the SiNWs devices.

	Implanted CL	Non-implanted CL
Back-gate control (in dry environment)	**p-type only** unstable operation	**p- and n-type** unstable operation
Front-gate control (in wet environment)	**p-type only** stable operation	**n-type only** stable operation

Table 4.5. *Obtained SOI transistor types from a lowly p-doped silicon layer depending on implantation status of the contact lines and depending on front-gate or back-gate operation.*

The SiNW chips still have some limitations that could be improved in a next chip design. First, the effect of the serial resistance of the contact lines is limiting the device performance especially for the 4×4 array with 6 SiNWs parallel per sensor spot. In the

second generation, this effect was improved by using single, small and long wires at each sensing point. However, with a shorter wire (less than 10 μm) the resistance of the contact line is still dominating at high V_{FG}. This effect can in future be overcome by several options: i) design the metal contacts closer to the SiNWs; ii) using a silicide for the contact lines; iii) increase the thickness of the top Si layer and use a longer etching time to minimize the size of the SiNWs. The second and the third options have an advantage over the first one, because the fabrication process could employ the high quality LPCVD oxide for passivation of the contact lines. The usage of LPCVD oxide for passivation is of general importance for a stable operation of the devices inside the electrolyte environment.

Second, the usage of a thick layer of SiO_2 as a hard mask for the TMAH etching resulted in a strong under etching of the BOX layer during the chip processing. The under etching of the BOX eventually leads to free-standing wires such that the ratio of the front-gate surface areas exposed to the liquid was different with different wire width. This effect has to be taken into account for future chip fabrications as well as for the electronic characterization, when a comparison of the device operation should be done.

The use of a protecting thin thermal grown oxide prior to LPCVD deposition of the passivation resulted in more reliable devices. However, the SiNWs had a trapezoid shape with two different silicon (100) and (111) planes. The gate oxide on the (111) plane was thicker than that on the (100) plane leads to a difference in the specific gate oxide capacitance of the devices with different wire width. With the smaller wires, the gate oxide was in average much thicker than on the larger wires, where the (100) plane was dominating. This effect was limiting the performance of the smaller wire. One could overcome this effect by using a thicker Si layer and using long etching times to achieve a desired wire diameter having only the (111) plane exposed. The second option would be to use the native oxide. The third option would be to use self-assembled monolayer of polymer acting as gate dielectrics as well as surface functionalization for direct binding of the probe molecules to the Si surface [52, 54, 61].

The threshold voltage of the devices from both designs for the front gate operation is about -0.7 V, which was much higher than initially expected. The high threshold voltage demands relatively high V_{FG} voltage applied for the chip operation, which limits the device operation as well as many cause side-effects like electrochemical reactions on the surface. One could reduce the threshold voltage by increasing the doping level of the SiNW in future fabrication processes.

Chapter 5. Applications of the SiNW arrays as biochemical sensors

In this chapter, the use of SiNW-FETs as chemical and biological sensors is presented and discussed. As shown in chapter 4, the SiNW sensors can be operated by both back-gate and front gate configurations. In related literatures, the back-gate configuration was normally used for the detection of charged molecules without front-gate control [53, 61, 70]. However, as shown above, the back-gate characteristics of the devices used in this thesis were not consistent. Disturbances of the electrolyte solution such as (partial) solution exchange can cause big changes of the electric signal, creating signal artifacts. Another disadvantage of the back-gate operation is that one needs to apply high voltages. The high back-gate voltages lead to instabilities of the devices throughout long experiments [61], as well as to difficulties in the development of portable electronic read out systems for the SiNW-FETs. For this reason, experiments in this work were carried out using front-gate operation with a highly reproducible signal as shown in chapter 4. Several experiments were further carried out with back-gate operation. However, the results of those experiments will not be shown in this chapter. Therefore, the gate-source voltage shown in this chapter always specifies the front–gate voltage (V_{FG}) applied through the reference electrode, which was immersed in the electrolyte chamber of the encapsulated chips. A

commercial electrochemical reference electrode was used for all the experiments to avoid any side effects that could happen by using a pseudo-reference electrode such as an Ag/AgCl wire or other metal electrodes (Au, Pt). The measurements were carried out with the both setups shown in figures 3.8 and 3.9.

5.1. pH sensitivity of the SiNWs

To investigate the pH sensitivity of the SiNWs, the transfer characteristics and output characteristics of the devices were carried out with different pH buffer solutions in the first experiments. The experiments were performed thoroughly with all SiNW chip types in both fabrication rounds. In order to avoid any degeneration effects, only new chip (not used before) were used for pH sensitivity experiments. The encapsulated chips were cleaned thoroughly before every experiment using the protocol described in section 3.4. The characteristics were first started with a solution of a value pH 2, and then the pH-value was step-wisely increased with an increment of 2 to a maximum of pH 10. In between solution exchanges, the chips were cleaned by deionized water and dried by Ar gas, before the new pH solution was introduced.

The typical transfer characteristics of a p-channel SiNW-FET measured with different solutions of pH values are shown in figure 5.1 in linear and logarithmic scales, respectively. As can be seen in this figure, the transfer characteristics shifted to lower voltages (less negative) from the left to the right with increasing pH-value of the solution. This effect can be explained by the change of the flat–band voltage of the SiNWs caused by the change of the surface charges at the oxide-electrolyte interface. When the pH value of the solution increase, according to the site-binding model [96], the hydroxyl group on the oxide surface donate a proton to the solution and leaving negative charge on the oxide surface as described in section 2.1.2. The surface potential change is related to the change of the surface charge at the oxide interface according to Grahame equation (equation 2.25). Consequently, the flat-band voltage of the SiNW change leading to the shifting of the transfer characteristics curves according to the change of the pH value. More details about the pH sensitivity of SiNWs will be later discussed. The shifting of the flat-band voltage extracted from the transfer characteristics curves were approximately 41 mV/pH in both the linear and the subthreshold regions.

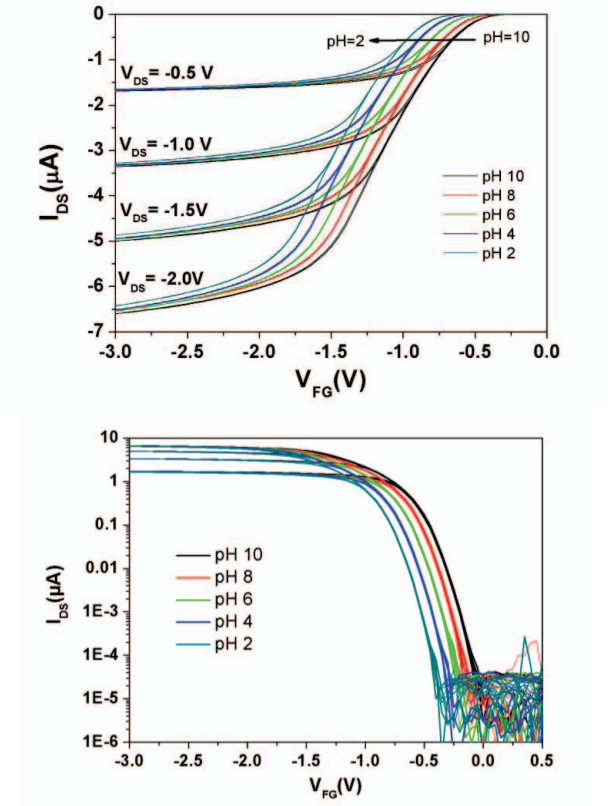

Figure 5.1 *Transfer characteristics of a p-type SiNW transistor measured with different pH-values solutions in linear scale (A) and in logarithmic scale (B).*

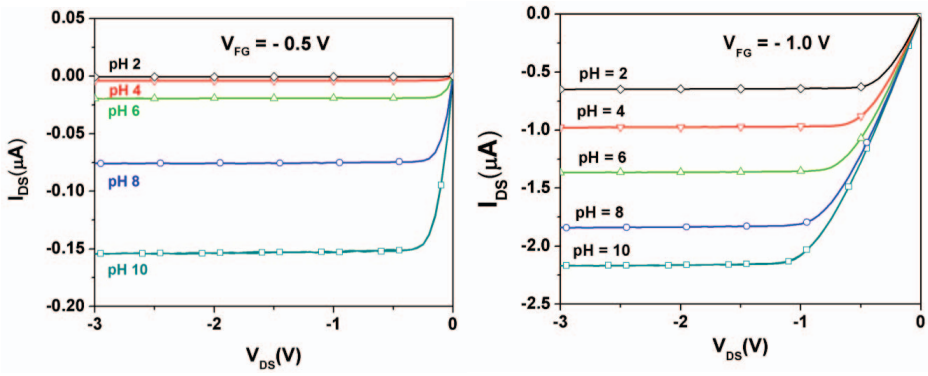

Figure 5.2*. Output characteristics of a SiNW transistor measured with solutions with different pH-values. The output characteristics was measured in the subthreshold regime (V_{FG}= -0.5 V) (left) and in the linear regime (V_{FG}- = -1.0 V) (right). The pH values were represented by the same color in both graphs.*

The output characteristics of the same chip as shown in figure 5.1 measured with different pH solution is shown in figure 5.2 for different V_{FG} (V_{FG} = -0.5 V (in the left) and V_{FG} = -1.0 V (in the right), respectively). As can be seen in these figures, at low value of V_{FG} (V_{FG} = -0.5 V, the figure in the left), the SiNW works in the subthreshold regime such that I_{DS} is exponentially dependent on the pH-value. At V_{FG} = -1.0 V the SiNW-FETs are working in the accumulation regime. In this case, the current magnitudes depend linearly on the pH value, when $|V_{DS}| > |V_{FG} - V_{TH}|$.

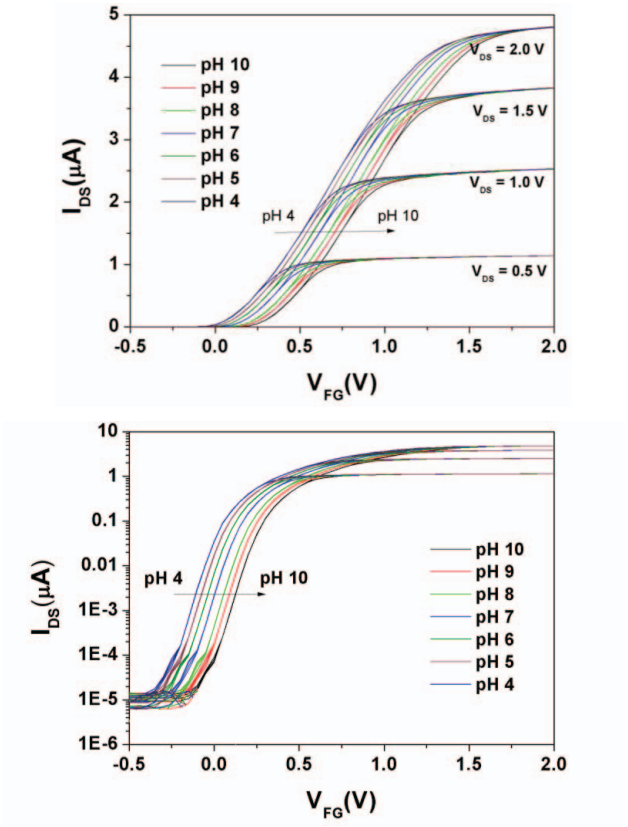

Figure 5.3. *Transfer characteristics of an n-type SiNW transistor measured with solutions of different pH-values in linear scale (A) and in logarithmic scale (B).*

Figure 5.3 presents typical transfer characteristics measured with an n-channel SiNW-FET chip (non–implanted contact lines) for pH solutions from 4 to 10 in a step of 1. As can be seen in these figures, for n-type transistor, the flat-band voltage shifts to higher voltage, (more positive) from the left to the right, with an increase of the pH-value. However, it has to be considered that V_{FG} is positive for n-type transistors, meaning that the increase of the pH-value leads to depletion of the charge carriers (electrons) in the channel. This effect is

contrary to the effect occurring in p-type transistors as shown in figure 5.1. The same value of 41 mV/pH of the flat-band voltage change was observed for the n-type SiNWs. Again, the flat-band voltage shifted linearly with the pH-value both in the linear and the subthreshold regions.

In general, the SiO_2 surfaces showed a drift in the output signal of the devices for long-time measurements [61]. However, the SiNW chips worked very reliably in all experiments. The transfer characteristics of the transistors did not show any change of the threshold voltage without changing the pH-value of the solution.

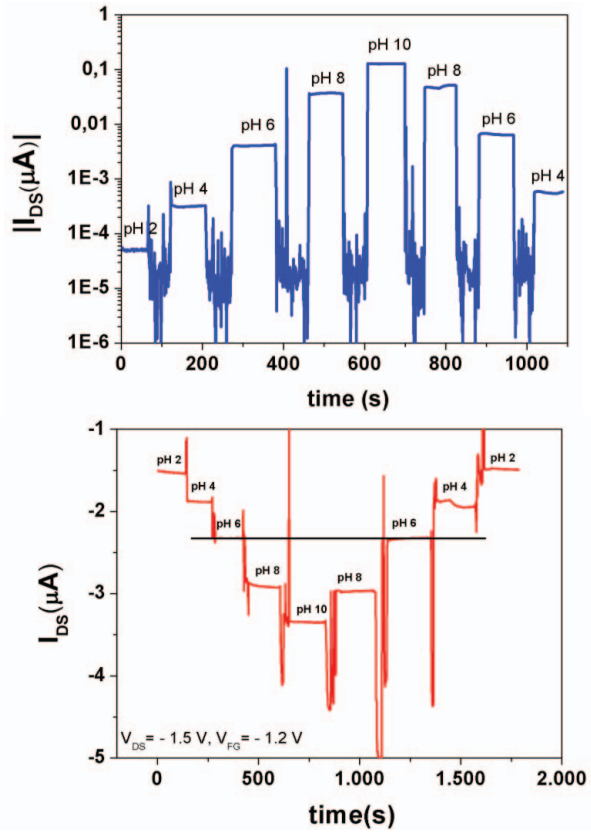

Figure 5.4. *Dependency of I_{DS} on the pH-value in the subthreshold region (left) and in the linear region (right).*

In the next step, real-time pH sensitivity measurements were carried out by recording the transistor current I_{DS} during an exchange of the electrolyte solution with a microfluidic system, which was integrated on chips as described above. The current I_{DS} were measured as a function of the pH-value by operating the device at a constant working point. This working point was chosen based on the transfer characteristics of the devices measured

with a pH solution of 2. The pH-value of the solution was altered starting from 2 to 10 and back to 2 with an interval of 2 – 3 minutes.

Figure 5.4 (top) shows the change of I_{DS}, working in the subthreshold regime (V_{FG} = -0.5 V, V_{DS} = -1.0 V). As can be seen in this figure, the I_{DS} is logarithmic proportional with the pH values in three decades from pH 2 to pH 10. When the SiNW operates in subthreshold mode, the change of I_{DS} is exponential proportional with the change of the applied gate voltage as:

$$I_{DS} \propto e^{q(V_{FG}-V_{TH})/mk_bT} \quad 5.1$$

where

$$V_{TH} \propto \Delta\Psi_S \quad 5.2$$

As a consequence, the surface potential at the gate oxide surface changes, $\Delta\Psi_S$, created by the different pH solutions cause a logarithmic scale change in I_{DS}.

During the solution exchange, the signal dropped back to a current of about 20-30 pA, which was the basic noise level of the measurement systems with Keithley 4000SCM. The signals that were measured during the solutions were introduced, showed a very low noise and almost no drift. For the pH-sensing in this measurement mode, the sensor showed a small electrochemical hysteresis between increasing and decreasing pH-values.

Figure 5.4 (below) shows the real-time pH sensitivity measurement above subthreshold voltage. The working point was chosen at maximum tranconductance of the devices at pH 7, V_{FG} = -1.2 V and V_{DS} = -1.5 V. When the SiNW operates in the regime, I_{DS} is proportional to square of the threshold voltage as:

$$I_{DS} \propto (V_{FG} - V_{TH})^2 \quad 5.3$$

and in this case the relationship between VTH and the surface potential is also as described in equation 5.2. Consequently, in this measurement mode, I_{DS} showed a linear behavior in relation to the pH-values as:

$$\Delta I_{DS} \propto g_m \Delta\Psi_S \quad 5.4$$

The results of the pH-sensitivity in term of flat-band voltage shifting of the different SiNW-FET are summarized in figure 5.5. Figure 5.5.A presents the results including the data of the two measurements shown in figure 5.1 and another measurement with an 80 nm device. Figure 5.5.B presents the pH sensitivity of a single-wire SiNW transistor out of the 28×2 arrays. One can clearly see that, when re-calculated to equivalent front-gate voltage changes ΔV_{FG}, the sensors exhibit the same pH-sensitivity, which was not depending on the operating point or device dimensions [75, 81].

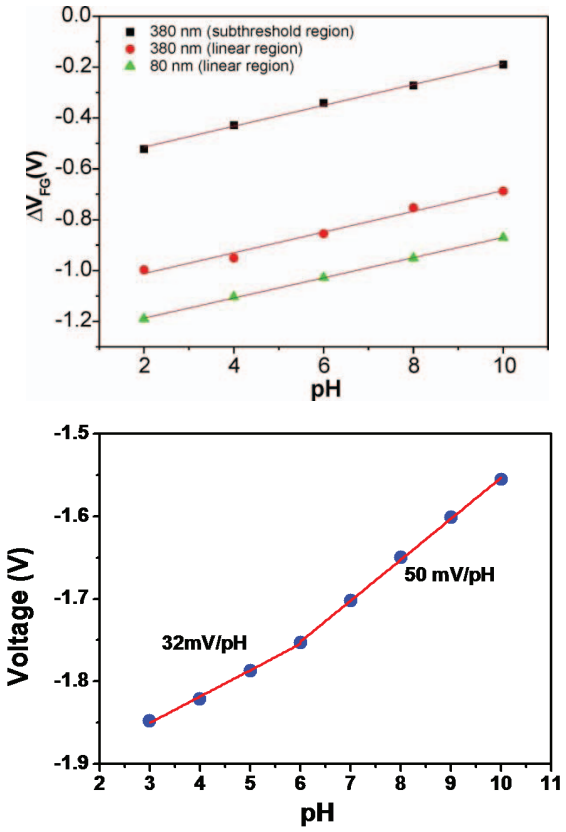

Figure 5.5. *Comparison of the two different pH-characterization measurements (operation in the subtreshold or the linear region). The sensors exhibited a sensitivity of 41 mV/pH, which is typical for a silicon oxide surface. With front-gate operation in both regions, the sensors showed a reproducible response independent of the nanowire size.*

In this study, the SiNW FET sensors were electronically operated similar to what is usually done with larger-scale FET devices used for ion-sensitivity measurements. With respect to the terminology used in this field, we can apply the basic equations used to describe the process of pH-sensing for the SiNW-FETs as well [189]. The threshold voltage V_{TH} of these devices (equation 2.1) is shortly described as:

$$V_{TH} = V_0 - \Psi_s \qquad 5.5$$

where V_0 is constant, Ψ_s is the effective surface potential, which is a function of the pH-value and the ionic charge q:

$$\Delta\Psi_S = -2.3\alpha\frac{k_bT}{q}\Delta pH_{bulk} \qquad 5.6$$

α is the so-called sensitivity factor, which depends on the geometry of the devices, environmental factors such as the temperature and primarily on the chemistry of the gate oxide surface. For an ideal case, the oxide surface has a maximum sensitivity factor α = 1. At room temperature, a maximum sensitivity of

$$\frac{\Delta \Psi_S}{\Delta pH_{bulk}} = -2.3\,\alpha \frac{k_b T}{q} \approx 59.3\,mV \qquad 5.7$$

can be obtained. SiO_2 is well known as a non-ideal surface for pH sensing. With a sensitivity of 41 mV/pH, the α value of SiNW devices is 0.69, which is typical for a SiO_2 surface [95]. As the results of this section proved, the pH sensitivity of our SiNW transistors does not depend on the size of the devices (cross-section) in contrast to what was reported in several articles with back-gate operation of SiNW devices [53, 61], and also does not depend on the working point of the devices. A reason for this could be that the diameter of our devices is larger (> 80 nm) than in other reports, where it was shown that the sensitivity of the SiNWs increases, when the diameter of the SiNWs reaches a value below 140 nm [184]. However, even with wires smaller than this critical value, the pH-sensitivity is similar to the sensitivity of larger devices. On the other hand, using the front gate with an electrochemical reference electrode our SiNWs showed a pH-response as expected from theory. Some other experiments concerning the pH-sensitivity were carried out with a Ag/AgCl pseudo-reference electrode showing that the pH response was not linear for the whole pH-value range (pH 2 to pH 12) and could even achieve high values of pH-sensitivity (~60 mV/pH) in the range from 4 to 8. However, when analyzing these experiments, the contribution of changes at the reference electrode-electrolyte interface with different pH solutions needs to be taken into account as shown in equation 2.1 for the threshold voltage of the ISFET device.

In pH-sensitivity experiments, two different types of hysteresis might occur. The first one is an electrical hysteresis, which might originate from electrical polarization of fixed charges inside the wire structure or at the Si/SiO_2 interface region. For the SiNWs fabricated in this work by combining nanoimprint lithography, TMAH wet etching and formation of a high quality gate oxide, almost no electrical hysteresis was visible in the characteristics. The measurements presented in figure 5.1, 5.2 all included forward and backward measurements, where both respective lines overlap. Thus, it can be concluded that no electrical hysteresis was visible, proving the high quality of the top-down processed SiNW-FET sensors. A second type of hysteresis in pH-value measurements can originate from incomplete changes of pH-solutions, especially in the continuous measurements

shown in figure 5.4, when measuring during forward and backward pH-value steps. This is mainly influenced by the geometry of the liquid cell, the method of solution exchange, and surface effects at the liquid-solid interface.

5.2. Detection of Ca^{2+} ions by the SiNW devices

A proof–of–principle measurement to detect Ca^{2+}-binding with a peptide-modified SiNW surface was performed to prove the one possible application of the SiNW sensors. The peptide was immoblized on the SiNW chip as already discribed in section 3.5. In this case, the peptide was covalently bound to the SiNW surface through the GPTES silane. The binding event between peptide and Ca^{2+}-ions is reversible since the ions can be washed away from the peptide by using a Ca^{2+}-free solution. When binding the Ca^{2+}-ions, the conformation of the peptides change, leading to a change of the dielectric constant of the peptide layer as well as the capacitance [164]. The binding of the Ca^{2+}-ions to the peptide increases the number of positive charges on the SiNW surface [127], leading to a change of the surface potential Ψ_s. Both effects lead to a change in the flatband voltage of the peptide-modified SiNW when binding with Ca^{2+} ions. For a p-type transistor, the binding event leads to a shift of the flatband voltage to more negative values according to equation 2.1. Figure 5.6 shows the change in the transfer characterisitics of a SiNW transistor in response to the binding of Ca^{2+}-ions to the peptides. The black curves represent measurements done in 0.01×PBS buffer for the peptide-functionalized SiNWs. The red curves show the measurments in 0.01×PBS buffer containing 40 µM Ca^{2+}. The binding of the ions to the peptide leads to a shift of the flatband voltage up to 100 mV to more negative. When the Ca^{2+}-ions were washed away using the same buffer as in the first measurements, the flatband voltage shifted back to the initial value as shown in the blue curves.

For real-time measurements during the binding process, the device was set to its operating point (V_{DS} = -1.2 V, V_{FG} = -1.0 V), and the drain-source current was recorded for two independent channels, addressing different SiNWs on the chip. The reference measurement was carried out with the same buffer solution to subtract any existing drift of the device. Figure 5.7 shows the raw data recorded during the addition of Ca^{2+}-ions (left) and the analysis signal after eliminate the drift (right) of the two different single SiNW on the 28×2 arrays.

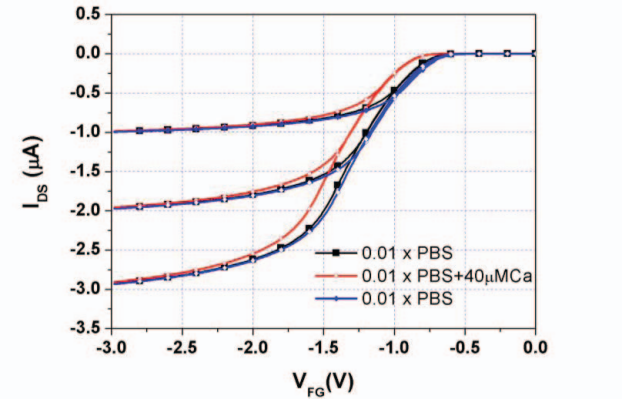

Figure 5.6. *Transfer characteristics for SiNW-FETs functionalized with CaM peptide. Black curves show the initial measurements in 0.01×PBS buffer. Red curves show the measurements after addition of 40 µM Ca^{2+}-ions to the buffer. Blue curves show the measurements in 0.01×PBS buffer after rinsing the chips.*

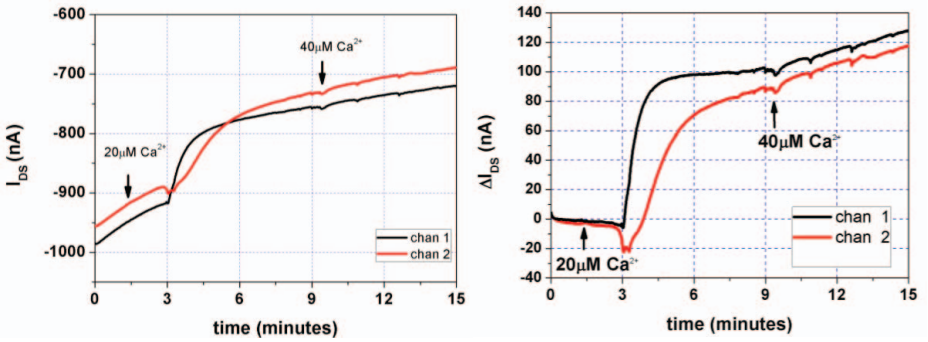

Figure 5.7. *Real-time detection of Ca^{2+} ions bind to a CaM peptide-modified SiNW. Recorded current signal for two independent transistors (Channel 1, Channel 2). The distance between the two channels were 500 µm. I_{DS} decreases after addition of Ca^{2+}ions to the electrolyte, when ions bind to the functional peptides and increase the threshold voltage leading to a decrease of current I_{DS}. The figure in the left presents the raw data of the measurement and the figure in the right shows the signals after drift correction using a reference measurement signals.*

When Ca^{2+} is added to the solution, the ions spread out due to diffusion until the electrolyte contains a homogeneous concentration of 20 µM. Once the Ca^{2+}-ions reach the gate surface of a recorded channel, they bind to the immobilized functional peptide. Hence, the accumulation of positive surface charges at the gate oxide depletes the holes in the p-type SiNW. Consequently, the drain-source current increases by approximately 100 nA

and saturates after 3 minutes after adding the Ca^{2+} ions. Moreover, one finds a time delay between the two recorded channels, which corresponds to the diffusion time necessary to overcome the distance between the two gates. A second addition of Ca^{2+} to increase the concentration to 40 μM did not lead to a further increase in the current, since the immobilized peptides at the gate electrode are saturated. Artifacts due to solution addition can be excluded, since the addition of Ca^{2+}-free electrolyte solution showed no effect. Control measurements, performed on a clean SiNW-transistor, given no indication for ion binding reactions (results not shown).

These results presented here are only primarily results illustrating that the peptide-modified SiNWs are highly sensitive to the binding of Ca^{2+}-ions. More experiments need to be done to determine the sensitivity limit of the devices as well as the selectivity to other bivalent ions such as Mg^{2+}.

These results, together with the results from other groups [127, 163], proved that SiNWs are capable to be used as chemical sensors for Ca^{2+}-ion detection and could also be used to study the biological activity of organisms by identifying biological processes such as muscle contraction, protein secretion, cell death, and development, where changes in Ca^{2+}-ions concentration are involved. This model of ion detection could also be extended for detection of other ions such as Pb^{2+}, K^{+}, Na^{+} in the environment as well as it can be applied to study cell activity.

5.3. Potentiometric detection of poly D lysine (PDL) molecules on the SiNW devices

The adsorption of PDL onto the SiNW surface changes the surface charge density at the oxide-electrolyte interface and leads to the change of the surface potential. PDL is positively charged at pH 7; its binding to the gate surface of the p-type transistors shifts the threshold voltage to more negative potentials. Consequently, it decreases the current I_{DS} at the working point.

Figure 5.8 shows the transfer characteristics of a SiNW sensor (130 nm × 20μm) before and after adsorption of PDL onto the SiNW gate surface. Measurements were carried out in 0.01 × PBS buffer, pH 7. As it can be seen, the transfer characteristic curves shifted to more negative values of about -130 mV related to a change in I_{DS} of 60 nA.

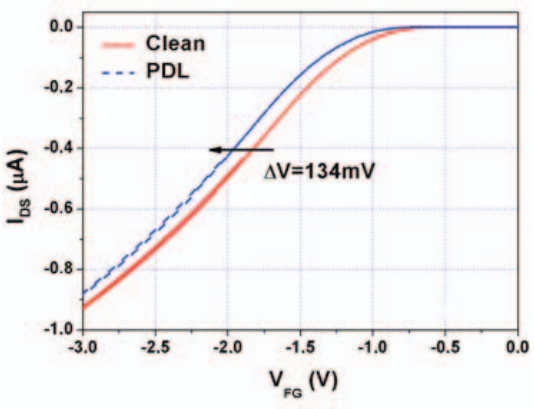

Figure 5.8. *Transfer characteristic of a single SiNW sensor (130 nm × 20μm) recorded before and after PDL adsorption on the surface. Both measurements were done in 0.01× PBS, pH 7. After PDL adsorption, the chip was rinsed several times with the same buffer before the measurement.*

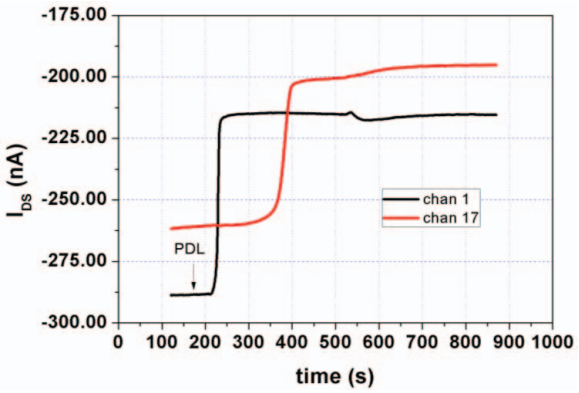

Figure 5.9. *Time dependence of the change of I_{DS} when PDL was introduced to the electrolyte solution It can be seen that the adsorption of PDL occurs quite fast that a diffusion of PDL molecules from channel 1 to channel 17 (500 μm) take about 170 s.*

The kinetic of the adsorption reaction of the PDL on the SiNWs was investigated by real time recording of the current change after injection of the PDL into the electrolyte chamber (0.01×PBS, pH 7). The PDL solution was diluted in the same buffer to a final concentration of 400 μg/mL. After a reference measurement for about 100 seconds, a volume of 10 μL of PDL solution was gently introduced the electrolyte at the edge of the chamber to achieve a total PDL concentration of 20 μg/mL. After PDL molecule diffused into the electrolyte and consequently adsorbed on the SiNW surface, the current decreased dramatically. Figure 5.9 presents the real-time measurement of the current change during

the adsorption of the PDL molecules onto the surface of the SiNWs. The difference in the time scale of the current change of the black and the red curves is due to the different distance of the sensor to the spot where the PDL was introduced. The distance between these two channels was 500 µm. A second addition of PDL to the electrolyte induced only a small change of the current. This means that the surfaces of the SiNWs were already saturated with PDL molecules. The results also indicated that with a PDL concentration of less than 20 µg/mL, the SiO_2 surface was already saturated

In the other measurements, after PDL was introduced into the electrolyte chamber, the same effects were observed. However, after reaching the minimum, the current slowly increased again on the channel close to the spot where the PDL solution was introduced (black curve). Meanwhile, in other channel the current slowly increased and stabilized at a minimum value (red curve) as indicated in figure 5.10. In this experiment, the second introduction of PDL to the solution did not cause any further change of the current. The increase again of the current on the channel 1 (black curve) after a minimum has been reached can eventually be attributed to a redistribution of the PDL molecules adsorbed on the SiNW surface to the solution due to the equilibrium condition. Whereas the other channel did not show such changes on the signal and equilibrium condition was reached due to the diffusion of PDL on the solution. In figure 5.10, the time scale between the maximum of the current for this two channels with a distance of 500 µm was about 530 s.

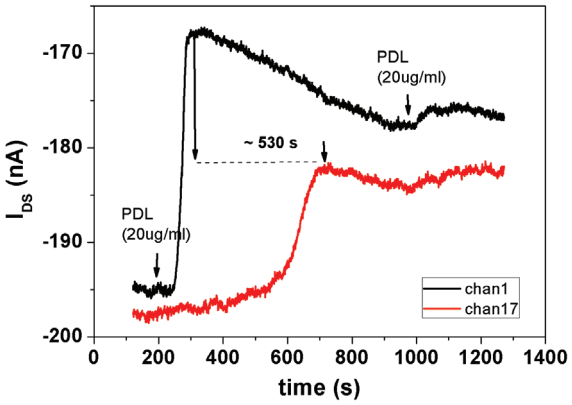

Figure 5.10. *Time dependence of the change of I_{DS} as PDL was introduced to the electrolyte solution*

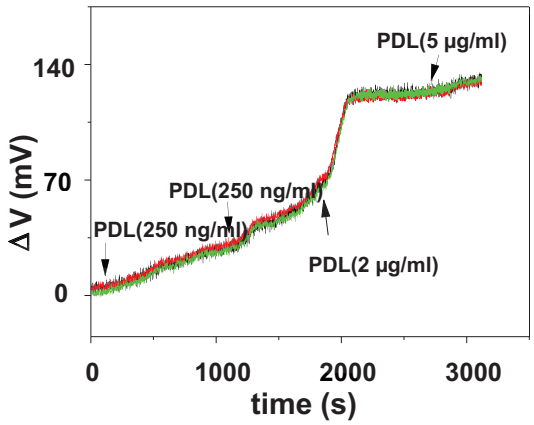

Figure 5.11. *Concentration dependence of the output voltage, when PDL solutions of different concentration were introduced to the SiNW surface*

Figure 5.11 presents a concentration dependence measurement of PDL adsorption. A low concentration of PDL (250 ng/mL) induced only a slight change of the output signal. When the concentration was increased to 2 µg/mL, the output voltage dramatically increased and reached a steady state after a few minutes. Further increase in the concentration to 5 µg/mL did not lead to a further increase in the output voltage. Consequently, the SiO_2 surface was saturated with PDL molecules at a concentration of 2 µg/mL.

5.4. Potentiometric detection of polyelectrolytes multilayer build up on the SiNW

Apart from the development of a sensor device for protein, DNA or other chemical and biological detection, a lot of other interesting questions might be addressed by the application of SiNW transistors as sensor devices. Among these, gaining a better understanding of the mechanisms involved in the adsorption of polyelectrolyte multilayers is an intriguingly discussed question in literature [191].

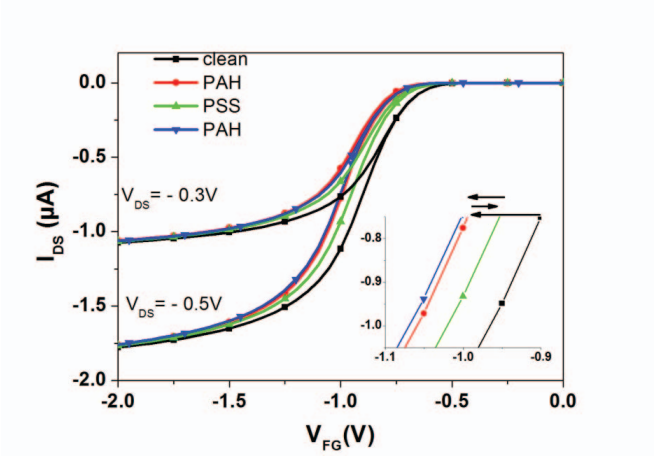

Figure 5.12. *Transfer characteristic of the SiNWs (6 wires in parallel, 130 nm × 3 μm) out of the 4×4 arrays recorded after adsorption of the first three layers of PEs on the SiNWs surface. The adsorption of positively charged PAH on the SiNW (red curve) lead to a change of 110 mV to more negative potential compared to the freshly cleaned SiO_2 surface (black curve). The adsorption of the negatively charged PSS onto the PAH layer shifted the transfer characteristics curve back to more positive potential at about of 40 mV.*

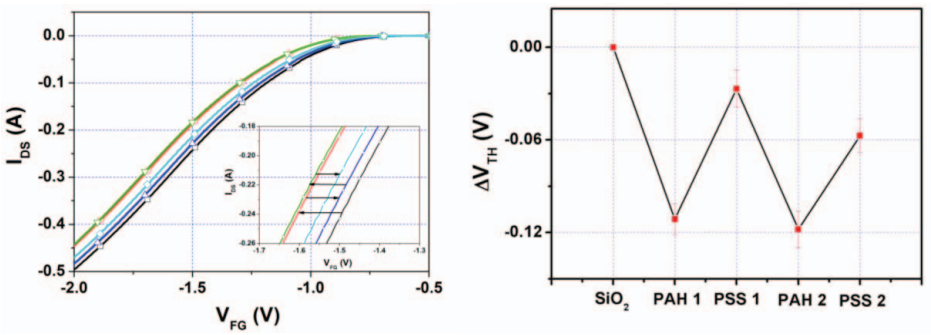

Figure 5.13*. Transfer characteristics of a SiNW from the second design recorded after each layer of PE adsorption on the SiNW surface. The adsorption of positively charged PAH onto the SiNW (red curve) lead to a change of 110 mV to more negative potential compared to the freshly cleaned SiO_2 surface (black curve). The adsorption of negatively charged PSS onto the PAH layer shifted the transfer characteristics curve back with a value of about 84 mV.*

In this thesis, polyelectrolyte multilayer composed of PAH and PSS were deposited through a buffer solution containing PAH or PSS onto the clean and fresh gate oxide surface. In between each layer, the sensor was rinsed with the pure buffer solution several

times. The buildup of polyelectrolyte multilayers was monitored by a change in the threshold voltage of the transfer characteristics of the SiNWs.

The transfer characteristics of the SiNW chips after deposition of each layer of PE is shown in figure 5.12 for the 4×4 arrays of the first chip generation, and in figure 5.13 for the 2×28 array of the second chip generation, respectively. After the first PAH adsorption, the flat band voltage of the chips was shifted 110 mV to lower voltage (more negative potential), respectively. This change was caused by the change of the charge density at the surface interface due to the positively charged PAH. This effect is very similar to the adsorption of the PDL layer above. The second adsorption of the negatively charged PSS shifted the flat-band back voltage to a more positive potential. In further adsorption steps, the shift in flat-band voltage alternated for the PAH/PSS adsorption due to the alternating charge type at the surface of the SiNWs. In addition, the change of the flat-band voltage of the 4×4 array chips after the second layer was about 40 mV, while with the 2×28 arrays chips, the second PSS adsorption lead to the change in the flat-band voltage of 80 mV. A further increase in the number of PE layers yielded a reduction in the signal response as described in previous publication for field-effect detection of polyelectrolyte adsorption [42, 82, 158, 171].

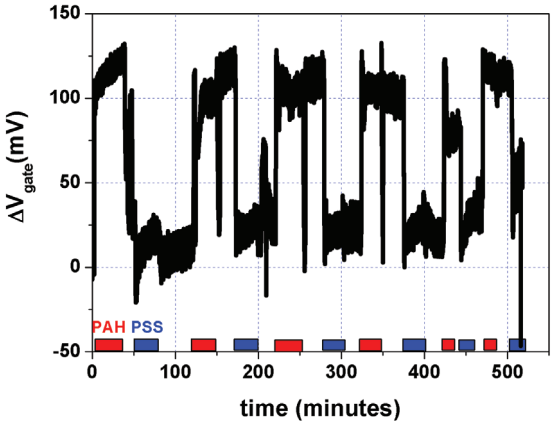

Figure 5.14 *The change of the gate voltage upon layer-by-layer adsorption of polyelectrolytes onto the SiNW surface. The graph shows a time-dependent measurement using a flow cell.*

Real-time observations of the flat-band voltage change upon buildup of PE multilayers on the SiNW sensors were carried out with a microfluidic system. The microfluidic cell was aligned onto the 2×28 array devices out of the second design. The solution was introduced by an external flow cell. The electrochemical reference electrode was fixed at the outlet of

the flow cell (figure 3.14). For the measurement the TTF box set up with a parallel 16 channel readout was used. Firstly, the transfer characteristics of the chips were measured in phosphate buffer and then the working point was set at the maximum of the transconductance value. To get a reference value for the output, pure phosphate buffer was flushed through the microfluidic chamber. After that, the pure buffer was exchanged to a buffer containing PAH (50 µM of PAH in 10 mM phosphate buffer, pH 5.5). Because PAH is positively charged at the pH value used, it was spontaneously adsorbed onto the freshly cleaned SiO_2 surface, resulting in a very large potential change of 110 mV. After 20 min, the cell was rinsed with the buffer leading only to a marginal signal change. Such effects were previously observed and can be attributed to rinsing off loosely bound molecules or reorganization in the respective sheet of the polyelectrolyte structure [42, 171]. After rinsing, the PSS solution (50 µM of PSS in 10 mM phosphate buffer, pH 5.5) was introduced leading to a signal change of about 80 mV. Further, alternating exchange of the PE solution caused an alternating output signal slowly reducing in amplitude (figure 5.14).

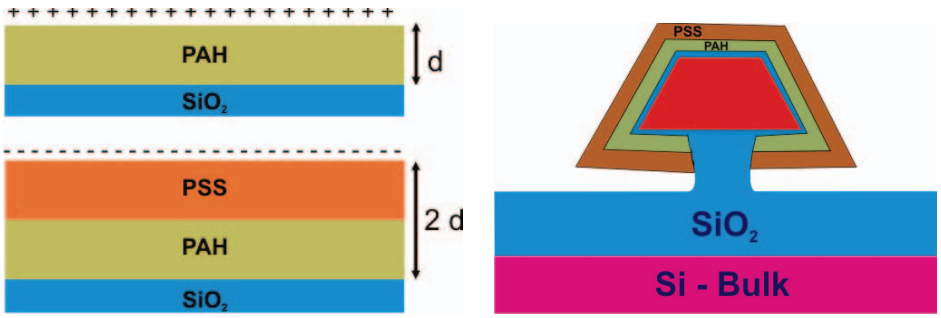

***Figure 5.15**. Capacitance model explain the buildup of the PE multilayers onto the planar devices (in the left)* [192], *and onto the SiNW structure (in the right).*

A model to explain the recorded field-effect signals during the PE multilayer build up was developed by several groups [171, 191, 192]. Several aspects contribute to the output signal of the field-effect devices. For instance, the changes of the flat-band voltage due to the charge of the polyelectrolyte on the surface; changes in the ion concentration inside the intermolecular spaces of the polyelectrolyte structure; presence of pores inside the PE multilayer, [42, 46, 171]; and the influence of capacitance changes, when layers of PEs are considered as an additional capacitance build-up on the surface [191, 193]. Figure 5.15 illustrates the capacitance model, where the PE layer is considered as a planar capacitor on the planar devices [192] and as wrapped-around capacitor on the SiNW structure.

5.5. Detection of biotin-streptavidin binding by the SiNW devices

In this section, the potentiometric detection of the biotin-streptavidin binding event is recorded by the SiNW devices. As already discussed in subsection 3.6, biotin-streptavidin is one of the strongest non–covalent biomolecular interaction in nature. Streptavidin has four binding sites for biotin. This property is used for targeted molecules in many different biomolecular detection technologies such as ELISA [194]. In some cases, this can also be used for immobilization strategy of ssDNA molecules onto the solid surface of DNA sensors. The detection of biotin-streptavidin binding normally is employed to boost the sensitivity of the SiNWs and also to understand the mechanism of the detection. The isoelectric point of streptavidin is 6.4 [172].

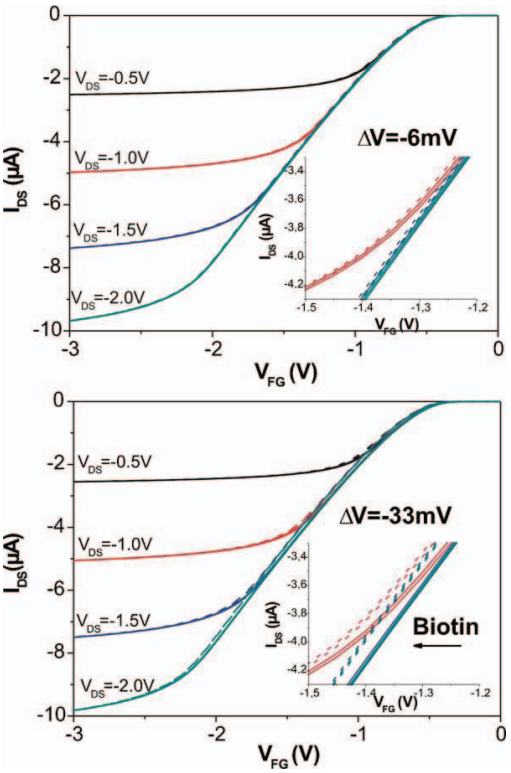

Figure 5.16. *Change of the flat-band voltage due to the immobilization of biotin onto the SiNW surfaces. The transfer characteristics were measured in a 0.01 × PBS buffer. The biotin immobilized onto the SiNWs was leading to a 33 mV shift (bottom graph), while on the reference channel of the same array without biotin immobilization, a shift of only 6 mV was induces(top graph).*

The electrical measurement in this work was carried out in 0.01× PBS buffer, pH 7. In this case the streptavidin molecules are negatively charged. In contrast to this, biotin is positively charged in this pH regime. EZ-link NHS–LC-biotin was immobilized on the SiNW surface as already described in section 3.7. The chip surface was modified by silanization with APTES yielding an amino-terminated surface. The covalent binding between amino groups to the NHS group was carried out in boric acid buffer at pH 8 for 2 hours [42]. The chip was then rinsed with the boric acid buffer and subsequently rinsed with deionized water to remove the unbound molecules and the remaining salt solution. Electronic measurements were carried out in a 0.01× PBS buffer solution.

Figure 5.16 shows the transfer characteristics of the SiNW before and after biotin binding to the surface [62]. As a result, the flat-band voltage shift to more negative potential indicated an accumulation of positive charges at the SiNW surface due to the binding of biotin. This binding resulted in a 33 mV flat-band voltage shift. The reference measurement of channels without biotin showed only a minor shift of the flat-band voltage of 6 mV. This result is indicating that the biotin was also partly adsorbing to the reference channel during the chip cleaning after the biotin immobilization.

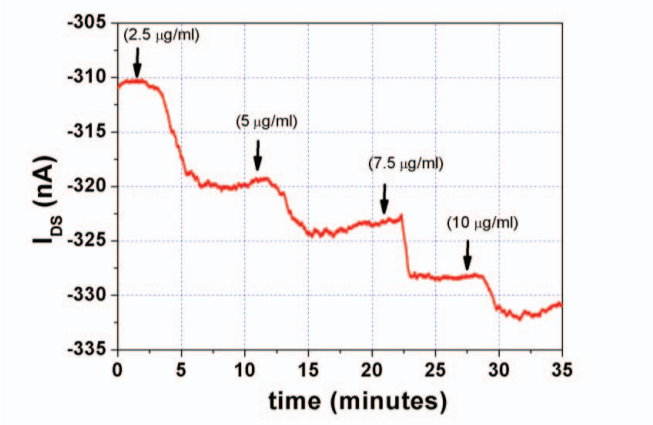

Figure 5.17. *Time dependent of the I_{DS} as a function of streptavidin concentration binding to the biotin on SiNW*

A real-time detection of the biotin-streptavidin binding was carried out by adding a appropriated concentration of the streptavidin to the buffer solution during the measurement. The SiNW chips were set to a working point and the current was recorded. Figure 5.17 shows the concentration dependence of the current change, when streptavidin was introduced to the electrolyte. The measurement started with pure 0.01 × PBS buffer. Then streptavidin was added to achieve a concentration of 2.5 µg/mL. After a certain time,

the streptavidin molecules diffused to the SiNW surface and were binding to the biotin layer on the SiNWs. Due to the negative charge of the streptavidin, the current I_{DS} increased about 10 nA. Further increase in the concentration of streptavidin was leading to a further increase of the current I_{DS}, however, the current increase was less compared to the first introduction. With 10 µg/mL of streptavidin the current I_{DS} increased about 30 nA compared to the pure buffer. This was related to a shift of 25 mV in flat-band voltage. After rinsing the chip with buffer and again measuring the transfer characteristic in pure buffer, the flat-band voltage shifted to 18 mV (figure 5.18).

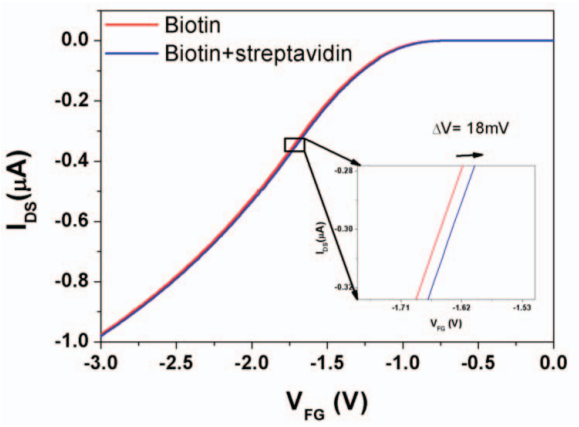

Figure 5.18. *Flat-band voltage shift due to the binding of streptavidin to the SiNW-biotinylated surface. The voltage shift was 18 mV to more positive potential due to the negative charge of streptavidin at pH 7. The red curve represents the measurement before and the blue curve presents the measurement after streptavidin binding. The chip was rinsed carefully to remove unbound streptavidin.*

To further study the sensitivity of the SiNWs, more measurements were carried out with the same type of chips. Real-time measurements were firstly carried out with pure buffer solution at the same working point. Then the streptavidin was introduced by pipette starting with a concentration of 0.25 µg/ml up to concentration of 10 µg/ml. The results of this measurement are shown in figure 5.19. As can be seen in this figure, after the first streptavidin was introduced to the electrolyte chamber and diffused to the SiNW surface (about 2 minutes) the I_{DS} increased and then slowly reduced to lower value. That could be the effect of reversible reaction of streptavidin and biotin at low ionic concentration. When the concentration of streptavidin is high enough in electrolyte, the binding process is much faster and stronger as illustrated by the larger change of I_{DS}.

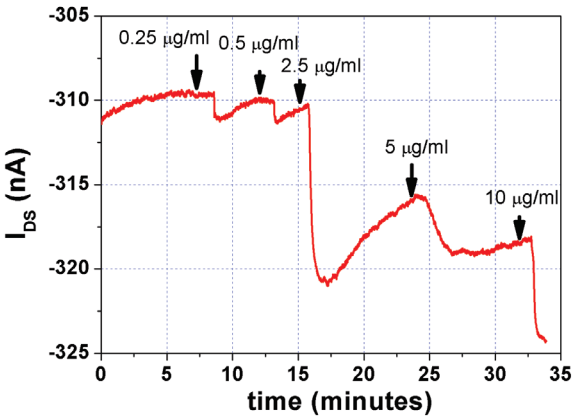

Figure 5.19. *I_{DS} as a function of streptavidin concentration. The measurement started at a concentration of 0.25 µg/mL of streptavidin with the large signal change of about 1nA*

5.6. Detection of DNA immobilization and hybridization

DNA molecules are negatively charged in electrolyte environment and can be detected by the SiNWs in a label-free fully electronic approach based on their intrinsic charges as already discussed in section 2.1 and 2.2 [52, 55, 70]. This section demonstrates the DNA detection with our SiNW chips in terms of DNA immobilization and hybridization on the SiNW surface.

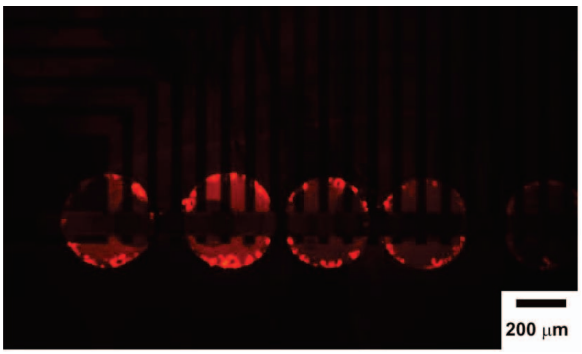

Figure 5.20. *Fluorescence image of cDNA hybridized with probes ssDNA on the SiNW sensor chips. The non-fluorescent probe DNA was immobilized by the GPTES silanization protocol and hybridized with a Cy3-labeled target cDNA.*

DNA was immobilized onto the SiNW surface through covalent bonding between amino-modified ssDNA as catcher molecules and the OH-terminated surface of the GPTES silane as described in section 3.7. Firstly, to verify the immobilization and hybridization process, a fluorescence labeled cDNA (Cy-3) was for the DNA hybridization process. The DNA

hybridization was carried out in 1×SSC buffer for 2 hours at room temperature. After that the chips were rinsed to remove the unbound cDNA on the chips surface and a fluorescence image was taken by using a fluorescence microscope. Figure 5.20 shows the fluorescence image taken after the DNA hybridization process. The fluorescence signal on the chip after DNA hybridization improved that the procedure for DNA immobilization and hybridization was successfully applied to the SiNW chips with the GPTES silanization protocol as reported before for a planar ISFET devices with SiO_2 surfaces [88].

In the next experiments, the electronic detection of DNA was carried out for both, the immobilization and the hybridization steps. The transfer characteristics of the SiNW were measured in the same measurement buffer (0.01×PBS, pH 7) using an electrochemical reference electrode at the front-gate side before and after the ssDNA immobilization step. The electronic detection of the DNA hybridization process was carried out in either by ex-situ or in-situ hybridization experiment as described in section 3.7.

DNA immobilization

Figure 5.21 presents the transfer characteristic of the SiNW chips before (black curves) and after the covalently immobilization of the ssDNA onto the SiNW surface (red curves). The upper graph presents the measurement after 2 hour of incubation and the lower graph presents the measurement after overnight incubation for the DNA immobilization process. Due to the negative charge of the ssDNA molecules in the electrolyte solution (pH 7), the threshold voltage shifted to more positive potential (lower value), which is typical for p-type SiNW transistors. The flat-band voltage shift was determined to 46 mV for the 2 hours incubation time and 146 mV for the overnight incubation time. The results indicated that the density of the ssDNA immobilization on the SiNW surface is dependent on the incubation time. According to the Graham equation (equation 2.25), higher density of ssDNA molecules lead to larger change in the flat-band voltage of the SiNWs. The reference measurements on the channel without spotted ssDNA showed no shift in the flat-band voltage. These experiments are interpreted in figure 5.22. A schematic of the ssDNA immobilization process was shown in the upper part of the figure. The ssDNA was immobilized on the different channels of the same chip at different time scales. In the first experiment, an ssDNA1 sequence was selected for immobilization on the upper part of the 28×2 SiNW array (for simplification these channels are called channel 1). The transfer characteristics for all channels on the chip were measured after this first immobilization process in 0.01× PBS buffer, pH 7. After that, an ssDNA2 sequence was immobilized on the whole SiNW array and the transfer characteristics were measured again for all channels

on the chip. The lower figure presents the transfer characteristics of the SiNW measured after each time of ssDNA immobilization. As it can be seen in this figure, there is a big shift of 150 mV in the flat-band voltage between the channel without ssDNA1 immobilization (black curve) and the channels with ssDNA1 sequence immobilization (green curve). After the ssDNA2 sequence was immobilized, the entire chip shows the similar flat-band voltage. The blue and the red curves present the transfer characteristics of the same channels as shown in the black and the green curves, respectively. Therefore, these results are indicating that after the first immobilization step the SiNW surface was already saturated with ssDNA1 molecules as it can be seen on the transfer characteristics of channel 2. There was no change in the flat-band voltage of the channel 2 after the second DNA immobilization (green and the red curves) visible.

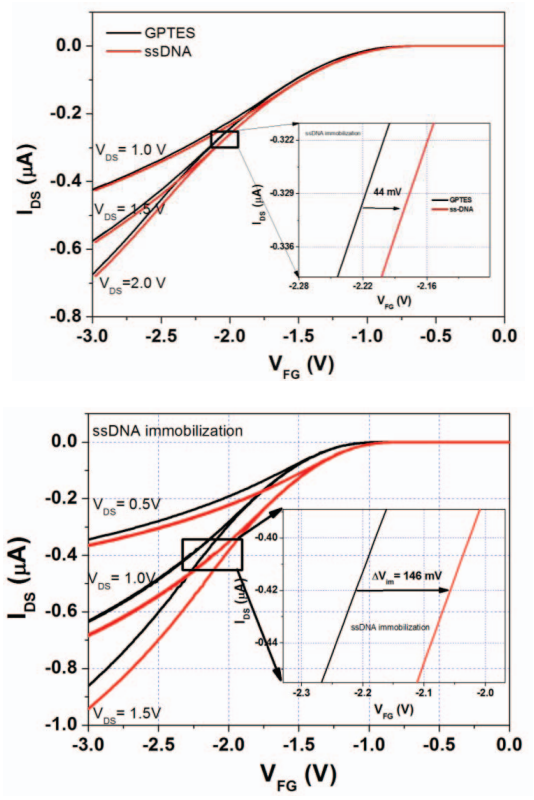

Figure 5.21. *Transfer characteristics of the SiNW devices before (black curves) and after ssDNA immobilized (red curves). The upper graph presents the result for the short incubation time (2 hours) and the lower graph presents the flat-band voltage shift for the long incubation time (overnight).*

Such kinds of measurements were performed many times. The changes in the flat-band voltage of the SiNWs after the DNA immobilization process varied for the different measurement. The resulting ΔV_{TH} value for the DNA incubation overnight varied from 100 mV to 150 mV very consistently. An explanation for this quite large variation of the ΔV_{TH} value could be that the spotting was not homogenous leading to a different density of the DNA on the surface of the SiNW.

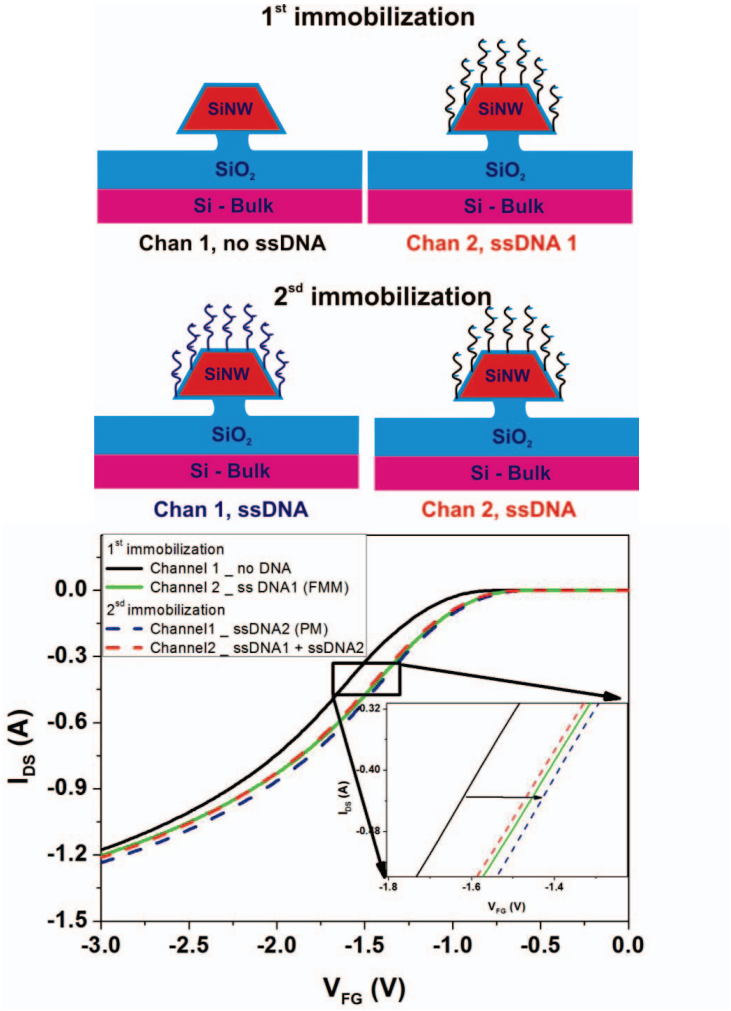

Figure 5.22. *Two steps DNA immobilization on different channels of the same SiNW array with flat-band voltage measurement at different times. The upper image illustrates the process steps and the lower graph measured flat-band voltage shifts after each ssDNA immobilization step.*

DNA hybridization

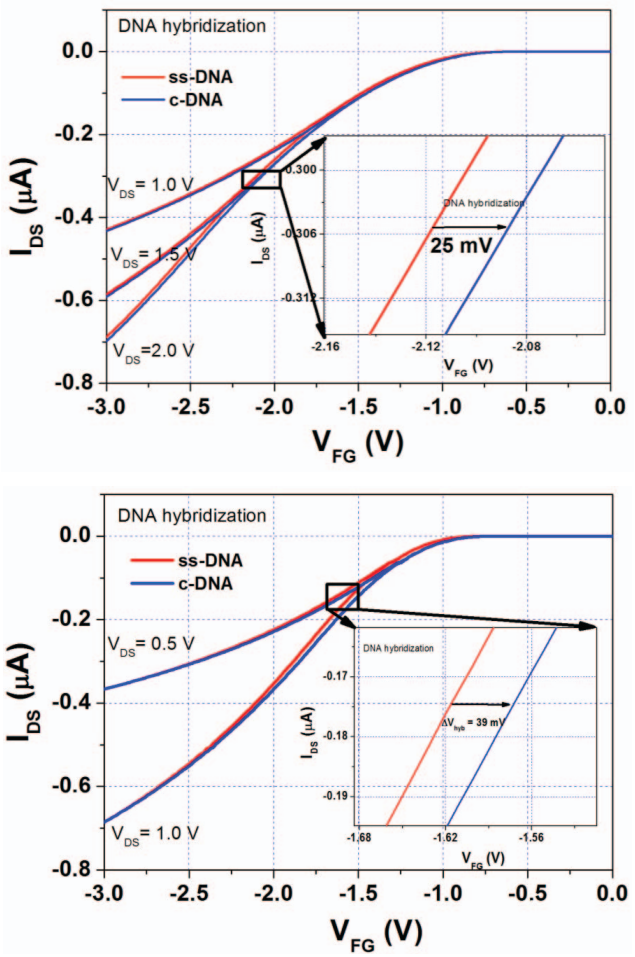

Figure 5.23. *Changes in the threshold voltage V_{TH} of the SiNWs due to the hybridization of cDNA. The red curves present the transfer characteristic before and the blue curves after the DNA hybridization.*

The detection of the DNA hybridazion was carried out many times as well either by ex-situ processes or real-time measurements. For the *ex-situ* detection, the DNA hybridization was carried out in 1×SSC buffer for two hours at room temperature [42]. After that, the chips were rinsed 3 times with the same buffer to remove the non-specifically bound cDNA molecules and then rinsed with deionized water to remove residual salt of the buffer solution. The transfer characteristics of the SiNWs were measured before and after the hybridization process in 0.01× PBS buffer soltuion. For the real-time detection, a working point of the SiNW chips were set to the maximum of the transconductance at certain V_{DS}.

The real-time measurements were carried out in 0.01× PBS buffer as well and the I_{DS} current during the DNA hybridization was mornitored. The cDNA was diluted in the same buffer and was added with a certain amout to the electrolyte solution.

Figure 5.23 presents two examples of *ex-situ* DNA hybridization experiements. In these figures, all the red curves present the measurement before the hybridization and all the blue curves present the measurement after the hybridization process, respectively. As can be seen in these figures, the flat-band voltage shifted to lower values (more positive potentials) after the hybridization process. This shift is also caused by the negative charge of the hybridizing DNA molecules. When the hybridization reaction takes place, the higher number of negative charges at the SiNW surface change the surface potential (Ψ_s) according to the Grahame equation (section 2.1.2). The change of the surface potential due to negative charges leads to an accumulation of hole carriers in the SiNW structure and the transfer characteristics shifts to a more positive potential. In our experiments, the voltage changes after DNA hybridization were in the range between 25 mV to 40 mV with the concentration of 500 nM cDNA as shown in figure 5.23. The measurements on the reference channel of the same chips without ssDNA immobilized showed no change in the signal.

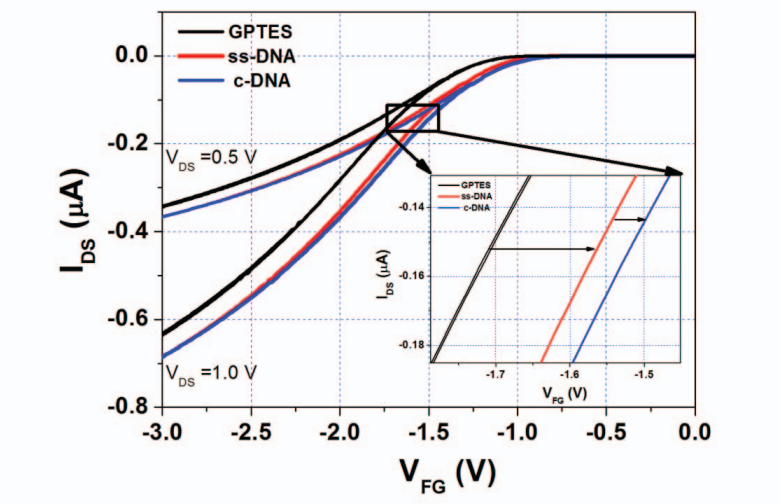

Figure 5.24. *Changes of the flat-band voltage of the SiNW chip due to DNA immobilization and hybridization. Due to the nagative charge of the DNA, the threshold potential V_{TH} shifted to lower values for the p-type SiNW transistors. The black curves are the measurement after GPTES silanization. The red curves and the blue curves are the measurements after ssDNA immobilization and cDNA hybridization, respectively.*

The total signal change recorded by the SiNWs due to DNA immobilization and subsequent hybridization processes are exemplarily presented in figure 5.24. The transfer characteristics were measured after GPTES silanization (black curves), after ssDNA immobilization (red curves) and after DNA hybridization (blue curves). All the measurement were carried out in 0.01×PBS buffer, pH 7. As can be seen in this figure, the transfer characteristic curves always shifted to the right (more positive V_{FG}) due to the nagative charge of the DNA molecules. The obtained signals are in agreement with the theoretical predictions [103, 105-108, 195].

In the following paragraph, some examples for the real-time detection of DNA hybridization are presented. The cDNA solution was introduced to the electrolyte chamber during the real-time recording of I_{DS}. The working point (V_{DS}, V_{FG}) was chosen at the maximum transconductance of the SiNWs obtained from the transfer characteristics measured after the DNA immobilization steps.

The measurement started with the pure buffer solution (0.01×PBS, pH 7) and was carried out for few minutes until the signal was stabilized and could be considered as the reference signal. The cDNA was then introduced into the electrolyte chamber by pipetting. To avoid the side effect such as the variation of the pH value and the salt concentration of the electrolyte, the cDNA was carefully diluted in the same measuring buffer (0.01×PBS, pH 7).

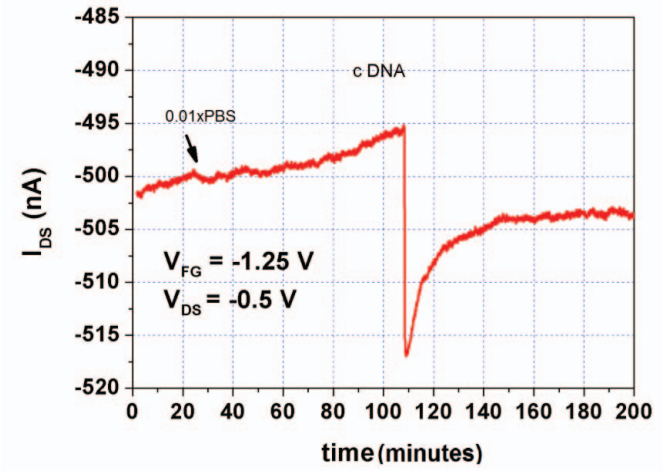

Figure 5.25. *Example one: A real-time detection of DNA hybridization. The probe ssDNA was immobilized onto the chip and the cDNA was added during the measurement. The ΔI_{DS} of 8 nA is related to a 15 mV change of the threshold voltage V_{TH}. The SiNW chip had a 300 nm width and 10 µm length.*

Figure 5.25 shows the real-time measurement of I_{DS} during the DNA hybridization reaction (example one). In this experiment, the value of I_{DS} remained unchanged, when first adding a reference buffer solution to the electrolyte chamber at 20th minute (first arrow). While after about one minute of adding cDNA solution to the electrolyte chamber (second arrow), the absolute current $|I_{DS}|$ increases dramatically and then decreases to a plateau after 30 minutes. The ΔI_{DS} was 8 nA and was related to a 15 mV change in V_{FG} in this particular measurement. This corresponds to the lower value as shown above for the *ex-situ* experiments.

The second example of a real-time DNA hybridization experiment is shown in figure 5.26. In this experiment, adding of a fully-mismatch DNA to the electrolyte chamber was not causing any change in the signal (blue curve). As soon as the cDNA was added to the electrolyte, $|I_{DS}|$ increased and was also stable after 30 minutes. The ΔI_{DS} change can be calculated to a change in V_{FG} of 17 mV.

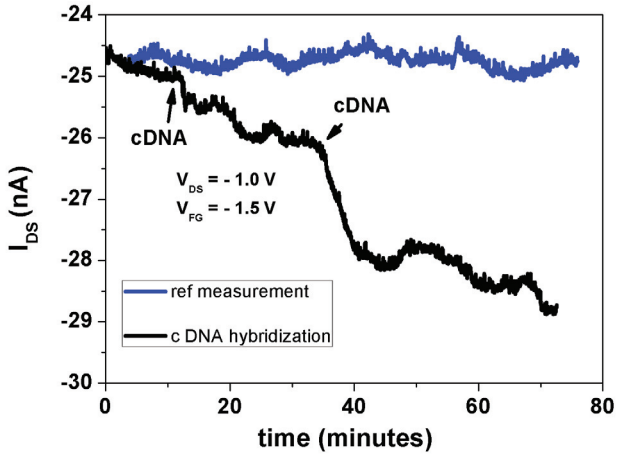

Figure 5.26. *Example two: Real-time detection of the DNA-hybridization process. The reference measurement is shown in blue and the signal of the DNA hybridization is shown in black. The two measurements present the same channel of a SiNW chip and were measured in a sequence.*

5.7. Summary and discussion

Table 5.1 summaries the measured results of the SiNWs presented in this chapter and compares to related results of previously works on the microscaled ISFET [42, 82, 171]

The presented results showed that the SiNW pH sensitivity of the sensors is reproducible and reaches value of 41 mV/pH. The pH sensitivity of the SiNW does not depend on the size of the wire as well as on the working point of the devices in contrast to what was reported in literatures with only back-gate operation [61]. In comparison to the microscale ISFET, the SiNWs showed higher sensitivity, however, the pH sensitivity of the SiO_2 surface of ISFET in literatures is in the range from 20 mV to 40 mV depends on the quality of the oxide layer [94, 95, 186]. It mean that with the front-gate operation of the devices, the pH sensitivity of the SiNW is the pH sensitivity of the SiO_2 surface or the quality of the SiO_2 surface and can be explained by the site binding model and obey the Nerntian equation. A low hysteresis of the pH sensitivity experiment indicated that the fabrication protocol of SiNW provided a high quality of the devices. The pH-sensitivity measurements in subthreshold regime open a new direction to employ the open-gate FETs for small-signal sensing, where a small change of surface potential creates a large change of transistor current I_{DS}. This effect is recently being employed to enhance the sensitivity of SiNW devices for biosensor detection [190].

Analytes	Threshold voltage change (mV) - absolute value	
	SiNW	Planar ISFET [42, 82, 171]
pH sensitivity	41 mV	25-30 mV
Ca^{2+} ion + peptide	100 mV	-
PDL	150 mV	
PEs	80-110 mV	10-20 mV
Biotin Streptavidin	33 mV 18 mV	- -
DNA immobilization DNA hybridization	40-150 mV 20-40 mV	1-10 mV 1-6 mV

Tabel 5.1. Obtained results for biomolecular detection. These results are compared with the micro-scaled ISFET devices.

The peptide modified SiNW was sensitive to detect the presents of Ca^{2+} in solution. As shown in section 5.2 the binding of the Ca^{2+} led to flat band voltage change up to 100 mV with the concentration of 20 μM. Two possible reasons explain the large change in the flat band voltage of SiNW: i) the change of the input capacitance due to the conformation of the peptide [184] and ii) the change of charge distribution at the interface due to the binding of the positively Ca^{2+} to the negatively peptide sequence. Real-time studies showed the Ca^{2+} diffusion inside the electrolyte solution as well as the binding kinetics of the ions to the fixed peptide on the substrate.

The adsorption of PDL onto the SiNWs led to changes in the threshold voltage up to 140 mV due to the buildup of a positively charged layer on the SiNW surface. The kinetics of the PDL adsorption was investigated by *in situ* measurements, which additionally gave information about the diffusion of the large molecules in the electrolyte solution. With fresh and cleaned surfaces, the PDL adsorption was fast and significantly stable. However, in all presented measurements, the PDL was only manually introduced into the electrolyte by using a micropipette, such that a diffusion coefficient could not be extracted. In order to gain more details about the diffusion and the adsorption of PDL on the surface, experiments employing a microfluidic system will be carried out in the future.

The signals recorded for the PE multilayer build up on the SiNW chips in this thesis are much higher than the signals previously recorded by microscale ISFETs [42, 82, 171] or on with SOI microwires [188]. The signals recorded with the nano-scale devices are higher compared to the micro-scale device as expected and described in other publications [22]. In the case of SiNWs, the surface-to-volume ratio is much higher compared to the standard ISFET devices leading to the higher sensitivity. This point needs to be taken into account to explain all contributions to the resulting output signal of the SiNW devices. For the SiNW structure, the gate surface is nearly wrapped-all-around the wires (figure 5.16, right) and the change of the gate capacitance is affecting the entire cross-section of the wire leading to a higher output signal compared to the planar devices. In addition, our chip fabrication protocol created very smooth surfaces of the SiNWs, thus, reducing the defects at the surface and, hence, increasing the sensitivity of the SiNWs. This structural effect can be used to explain the higher output signals for the protein detection as well as for the DNA detection as shown below.

In this work, the SiNWs were sensitive to detect protein molecules such as the biotin-streptavidin binding. The biotin molecule bound to the amino-modified SiNW surface which led to a 33 mV change in the V_{TH} while a value of 18 mV was achieved when

streptavidin molecules bound to biotinylated SiNW. The concentration dependence of this detection was investigated and a large signal change was visible at very low concentrations of streptavidin (0.25 µg/mL). However, the measurement was carried out at pH 7 close to the isoelectric point of streptavidin. The output signal could be enhanced if the pH of the solution was increased to values different from the isoelectric point. In addition, measurements with a pH solution around the isoelectric point will give more information about the activity of the protein in future.

The label-free, fully-electronic detection of DNA was demonstrated by the SiNW transistors. The immobilization of ssDNA on the SiNW led to large changes of up to 150 mV or even higher for a longer incubation time and 45 mV for a shorter incubation time on the transfer characteristics. These results indicated that the incubation time affected the density of the probe molecules on the surface. For the covalent bonding, especially on the GPTES surface, the negative charge of the surface caused by the opening of the epoxy ring eventually creating a repulsive force to the probe DNA, making it hard for the DNA to approach the surface. In addition, a large variation of the flat-band voltage shift was observed after DNA immobilization. This may be caused by the non-uniform spotting procedure of ssDNA onto the GPTES surface. Due to hydrophobic properties of the GPTES surface, the droplet of DNA solution can eventually move on the surface leading to a different density of the probe DNA on the silicon nanowire.

The label-free detection of the DNA hybridization was also demonstrated by the SiNWs. For the *ex-situ* detection, the output signals were in the range from 25 mV to 40 mV for DNA concentration of 500 nM. The hybridization reaction was taking place inside a high salt concentration buffer electrolyte. In this case, the negative charges of the DNA molecules are compensated by the cations in the buffer solution. Hence, the electrostatic repulsion between the probe and the target DNA is reduced to minimum and the target DNA can easily form a double strand with the probe DNA on the SiNW surface. In contrast to this, the *in-situ* measurements in a low salt concentration of the buffer solution were not very reliable. The observed changes in the signals were not reliable. Following effect could be the reasons for this behavior. Firstly, at a low salt buffer concentration, the DNA charge is not fully compensated by the counter ions. The electrostatic repulsion of the two single stranded DNA molecules is slowing down and reducing the probability of the hybridization process [52]. In addition, the GPTES surface is also negatively charged, which even increases the electrostatic repulsion between the surface and the target DNA. Secondly, the DNA hybridization changes the local concentration of the electrolyte by

redistribution of the ions at the interface or inside the inter-molecular space [108, 171]. Negative charges of DNA on the surface attract a higher number of positive ions, which modify the interface properties. This effect also results in a change of the surface potential and contributes to the total change of the output signal. Thirdly, the DNA hybridization is a reversible process which depends on several environmental properties. Eventually such side effects can lead to a degradation of the signal. Furthermore, the long-time measurements of the SiNWs can introduce a local heating effect on the SiNW [196] which could also lead to a denaturation of the double strand DNA.

Nevertheless, in comparison to the results of the DNA detection, that have been done in our group with the standard microscale ISFET [42, 46, 82], the output signals of the SiNWs are generally much higher in both immobilization and hybridization experiments. These results prove that the SiNW devices are much more sensitive than the micro-scale device due to the high surface-to-volume ratio as well as the device geometry. In future design, a further downscaling of the SiNWs and using suspended NWs can eventually lead to even more sensitive detection of charged biomolecules.

A general conclusion about the sensitivity of the devices is that the SiNW devices are more sensitive than the ISFET in term of the threshold voltage shifting. The PEs multilayer and the DNA immobilization and hybridization experiments were carried out in the nearly same protocol as previously experiments of the ISFET. In this case, the surface density of the biomolecules or the surface charge on the SiNW and ISFET should be similar. According to the Graham equation in chapter 2, the surface potential is related to the charge density on the SiO_2 surface. Applying this theory to the ISFET and the SiNW, one could expect that same signal is achieved for both kinds of sensors. However, as shown in table 5.1, the SiNW presents 8-10 times higher than the ISFET. The detail explanation for this effect was not yet established in the frame of this thesis.

Chapter 6. Conclusion and outlook

6.1. Conclusions

In this thesis, a novel approach for the wafer scale fabrication of the SiNW arrays for the sensor application was established and the devices showed much higher sensitivity compared to the normal microscaled ISFET. With the fabrication techniques that combine the novel nanoimprint lithography and TMAH etching of the Si, a large amount and highly reproducible of the SiNW-FET chips were fabricated. The chips were design in a large arrays posse a possibility of the reliable SiNW on chip as well as from chip to chip on the same wafer. The chips fabrication process was established create the reliable process from wafer to wafer. Nanoimprint lithography was employed to fabrication of the SiNW chip due to the high throughput. With this method, the whole 4 inch wafer was structured with a massive of chip in one step of replication structures from the imprinted mold. By optimization the process, we have overcome the proximity effect of the nanoimprint lithography such as the inhomogeneous of the residual layer and achieve combination of the nanosize of the wire and microstructure of the contact line on the same chip. The optimization was considered in two terms: Control the etching process of the residual layer by the RIE and redesign the arrays has a homogenous distribution of the cavities and the

structures. By these optimization we have achieve almost 100% successful of the process with the smallest resolution of 100 nm in our process.

The wet chemical etching of the Si with TMAH transfer the NW structure its self from the hard oxide mask on top of the Si layer. By using the SOI wafer, the Si layer was confined in between the top hard mask oxide and the BOX. Both of these acts as the etching stop so that the etching of Si was controlled only in the lateral way and create a trapezoid shape cross-section. By this approach, the size of the SiNW is tuned by different etching time. In our process, a SiNW with bottom of 60 nm with the length up to 40 μm was achieve and reliable. The thin top silicon layer was used as contact line towards the nanowires in the center of the chip, so the process was enable employed the LPCVD process to passivate the contact line for stable operation in a liquid environment. The performance of the SiNW was enhanced by boron ion implantation on the contact line and subsequence annealing to reduce the serial resistance and reliable operation. A high quality of the gate dielectric was applied by growing a thin layer of the SiO_2 by dry thermal oxidation at 820^{o}C with a thickness of 6-10 nm.

By this protocol that combine the nanoimprint lithography, TMAH etching with a conventional microtechnology, the process was establish at the IBN, Research Center Juelich and several processes were run though reproducible and reliable. Several layouts were tested through these processes. In the first design, beside the 4×4 arrays of the SiNW with the different wire width was fabricated for the measurement shown in this thesis, a 16×16 and 32×32 arrays was successful fabricated to boost the process and can be used for further application. In the second design, the array was designed in two line, each line consists of 28 individual SiNW addressed. The width of the wire was 200 nm or 400 nm with the length are 5 μm, 10 μm, 20 μm and 40 μm. In this process, an ultra-density arrays (128×128) was also successful fabricated on the same wafer. We have achieve the process improvement through the first to the second process in term of the smooth surface by avoid direct deposition of the LPCVD layer on the SiNW surface.

The SiNW was characterized carefully in term of surface topography and electrically. Thanks to the TMAH etching, a very smooth surface of the SiNW was achieve and ensure the low defect or low trap charge at the Si/SiO_2 gate interface lead to the good electronic characteristics of the transistor. The second design (28×2 arrays) creates a nearly planar SiNW arrays and avoid the barrier high of the contact line passivation that can be easy integrated to the microfluidic systems [81] and also create better cell adhesion [185].

The electronic characterization was carried out with the back-gate and front–gate configuration. Without the implanted contact line the SiNW shows a tri-mode operation with the back gate (accumulation, depletion and inversion) as p-type transistor at negative $V_{BG,}$ and n-type transistor at positive V_{BG} while with the front gate operation, the SiNW behave as n-type transistors. This effect was explained by the fixed charge at the oxide silicon interface and also the contribution of the Schottky contact at the metal-low doping Si. On the other hand, the SiNW behave only like a p-type transistor both by back gate and front gate operation with the chip was highly implanted by boron ions on the contact line.

The back gate operation without the potential control on the front gate was not stable in our measurement while the front gate operation was very stable and reproducible. A combination of the back gate and front gate indicated that the front gate was much stronger than the back gate due to the high surface to volume of the nearly wrapped all-around of the front gate in electrolyte.

The electronic characterization also indicated that the sensor utilizing a front-gate contact via an electrochemical liquid junction referent electrode were mandatory for the stable and reliable operation of the SiNW-FET devices.

The pH sensitivity of the devices was measured in the subthreshold operation regime and in the above threshold regime. In both cases, the pH sensitivity of the devices were 41 mV/pH as expected when using a silicon oxide surface. We also released that the pH sensitivity is independent from the size of the nanowire with the front gate operation.

In term of biosensor sensitivity, the SiNW show much higher sensitivity compared to the micro scale ISFET. The sensitivity of the devices was tested with the model of the multilayer buildup of the charge electrolyte on the surface. In this case, the first layer adsorption of the positively charged polyelectrolyte (PAH) or PDL lead to the change of the flat band voltage proximately of 120 mV to high value (p-type transistor). A second adsorption layer of negatively charge polyelectrolyte creates a change of 80 mV to lower value. These values are 6-8 times higher than the results of the same experiment with the microscale ISFET devices [42, 82, 171].

The SiNW also demonstrated as a sensitive sensor plat form for the protein, DNA or ion detection. The Ca^{2+} ion binding to the CaM peptide on the SiNW surface lead to a change of 100 mV on the flat band voltage with the concentration of Ca^{2+} is 20 µM. The binding process is reversible and after remove the Ca^{2+} from the electrolyte, the flat band voltage

comeback to the initial value. The binding of the streptavidin to the biotinylated SiNW was demonstrated and can be served as model for the protein detection. In this case, the streptavidin binding lead to the change of 18 mV on the flat band voltage of the device to lower value at pH 7 close to the isoelectric point of the streptavidin.

SiNW was also demonstrated as sensitive DNA sensors. We develop a new surface modification method for the DNA immobilization that used silanization with GPTES. By this approach, the amino-modified ssDNA was directly covalently bound to the silane without cross linker step, this reduces the time consuming and the cost of the DNA immobilization process. The GPTES silane can also be used for direct immobilization of peptide or protein on the surface.

DNA experiments were carried out based on potentiometric read out. The ssDNA immobilized on the SiNW lead to a change the flat band voltage of 40 mV with a low density of ssDNA and up to 150 mV with a high density of ssDNA. However, there are a variation of the flat band voltage change in these experiments from chip to chip and also from the experiments to experiments and difficult to evaluate the sensitivity of the different sensor size. The DNA hybridization leads to the change of 20 mV to 40 mV in the flat band voltage in the ex situ hybridization. The real-time detection of the DNA hybridization was demonstrated with a clear change in the signal due to this process.

6.2. Outlooks

As discussed above, the fabrication process for the SiNW – FET arrays was established, however, the devices still can be improved in term of mechanic stabilities and electric performance.

The variations of the wire width can be eliminated by fabricating higher imprint mold quality. In our case, the mold was fabricated by the e-beam lithography and RIE. By this process, the edges of the structures are uneven and become worst in the process flow. This effect can be avoid by fabricating the mold based on the simple wet-chemical anisotropic etching of the structures on the Si (110) wafer or on the SOI (110) wafer. The anisotropic etching of silicon on this wafer creates a vertical wall to the surface with the atomic roughness compared to few nanometer of the dry etching.

The use of thin Si layer as contact line lead to high serial resistance and affect to the device performance and maybe the sensitivity of the device as well as the device noise. The contact line resistance can be reduced by bring in a metal contact line close to the SiNW.

However in this case, the use of LPCVD process for passivation layer is impossible and it has to be used the PECVD process. The best case is employed silicidation process of the Si contact line such as Ti-silicide or Co-silicide. By this approach we achieve both requirements: the small resistance of the contact line and possible to employ the LPCVD process for the passivation layer. A further downscaling of the SiNWs and using suspended NWs could eventually lead to even more sensitive detection of charged biomolecules.

In this thesis, several proof-of-principles experiments were carried out in term of the biomolecular detection. In the feature, the measurements with the different concentration of the biomolecules need to be carried out to boost the sensitivity of the devices. Based on the detection of the DNA molecules and the biotin-streptavidin binding, this flat form can extend to detection many object such as the immune assay, enzyme, microorganisms, virus and small molecular or to study the cellular signal such as the signal propagation of the action potential in the neuronal network.

Based on the Ca^{2+} ion detection, the sensor can also possible to use as chemical sensor to detect other ions such as Na^{+}, K^{+} or many other ions. On the other hand, this platform can be used to enhance the signal of the cellular response such as the increase the action potential signal of the cell or study the apoptosis process that the specific ions are released from the cell body to the extracellular environment or uptake from the solution to the cell body lead to the change of the local ion concentration.

Thus, the work presented in this thesis could provide the new platform for the sensing across a large number of fields. Label-free sensing integration with high sensitive transducer based on electronic read out should greatly decrease costs in numerous clinical, public health and basic research application.

Appendices

A. Chip designs and fabrication process

A.1. Chips design

A.1.1. First chip design

In the first design, all structures are 3 µm long and are available in four different widths (1 µm, 500 nm, 250 nm and 100 nm). The width used on a specific chip is indicated by a number on the lower left corner 1, 5, 2, 01 respectively.

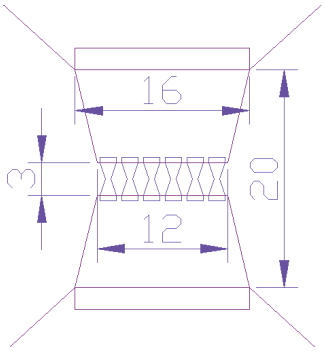

Figure A.1: *A detail description of a gate area*

4×4 arrays with common source:
This is the most widely used version, the structure of which is shown below. The pitch of the active sites is 200 µm.

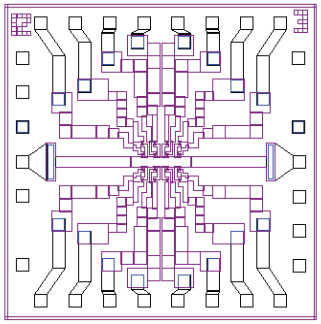

Figure A.2: *Layout of a 4x4 arrays with common source*

16×16 arrays with crossbar addressing:
This is a test version to see whether the concept of directly addresses active areas (pitch 100 µm) is feasible for our devices. It only exists as one type with 500 nm wide, triangular wires (structure below).

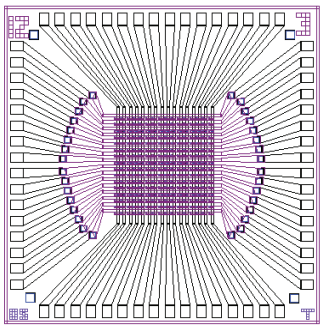

Figure A.3. *Layout of a 16x16 arrays with crossbar addressing*

32×32 arrays with crossbar addressing:
Also a test design with an even higher density of active areas (pitch 50 µm). Due to the reduced width of leads a higher contact resistance is expected. That is why the NWs are packed more densely here (250 nm width, 500 nm distance), which results in 14 NWs per active site.

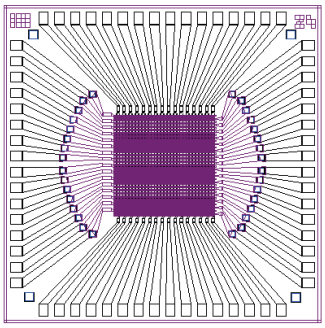

Figure A.4. *Layout of a 16×16 arrays with crossbar addressing*

For simplicity in all cases the ones with gate width 12 µm and length 3 µm are used as the existing masks for implantation and passivation always fit these dimensions, even when intended for different ones. In the main variations the pitch of the wires is 2 µm, which results in six wires per active area.

A.1.2. Second chip design

28×2 arrays with single wire and common source

The second chip designs were mainly based on 28×2 arrays as discussed in section 3.1. The widths of the wires were 200 nm and 400 nm (mask measure), the lengths of the wire were 5 µm, 10 µm, 20 µm and 40 µm. The pitch between two lines is 500 µm for all the 28×2 arrays type. On a specific chip the length of the wires was indicated at the left bottom corner and the width was indicated at the right bottom corner.

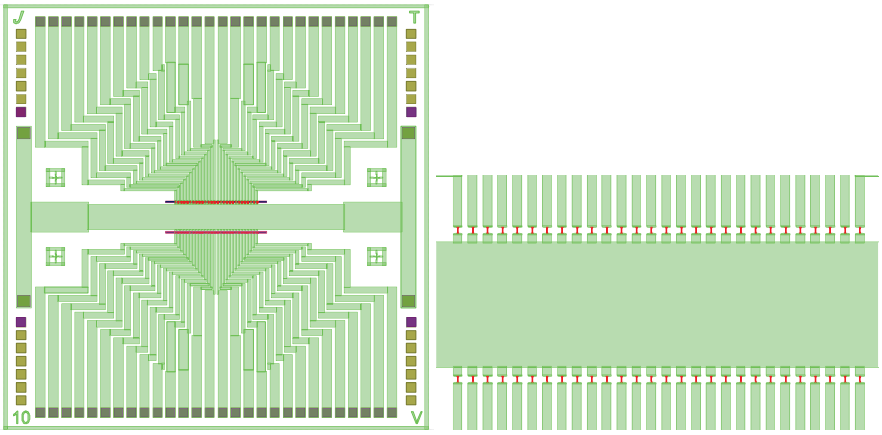

Figure A.5. *28 ×2 arrays with a common source:*

28×2 arrays with multiwires and common source

The design was based on 28×2 arrays. The length of the wire was fixed at 10 µm. The number of wires was from 1 to 5 wires on identical gate. The upper line has the wire widths of 200 nm and the lower line has the wire width of 400 nm.

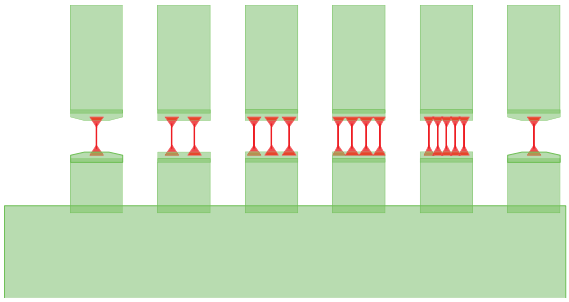

Figure A.6. *Number of wires variation on the test chips*

4×4 arrays with single wire and common source

The chip was design based on the standard 4×4 arrays ISFET design at IBN. There is a single wire at each gate. The wire length was fixed at 5 µm and the width was fixed at 400 nm. The pitch of the gate is 200 µm.

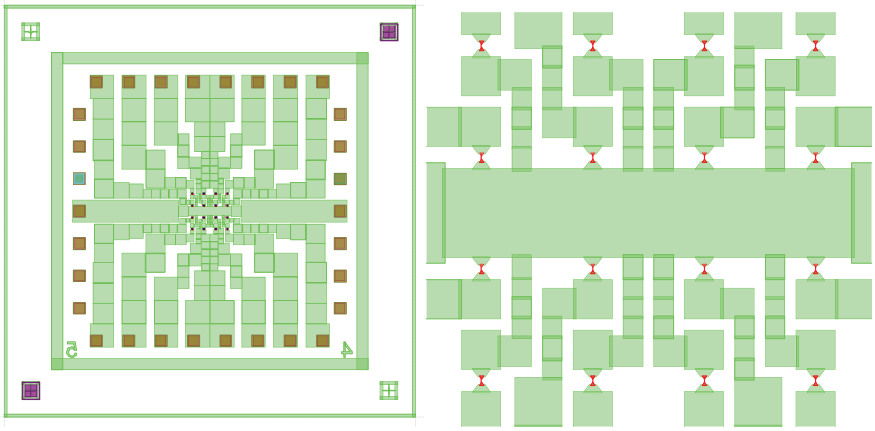

Figure A.7: *Layout of a 4×4 arrays with common source on the second design*

128×128 arrays with crossbar addressing

The high density arrays were added to boost the process as well as for further application like multiplexing detection. The wire width was fixed at 400 nm and the wire length was fixed at 5 µm. The pitch between the active areas is 25 µm. Each side of the chip has 64 contacts for the crossbar.

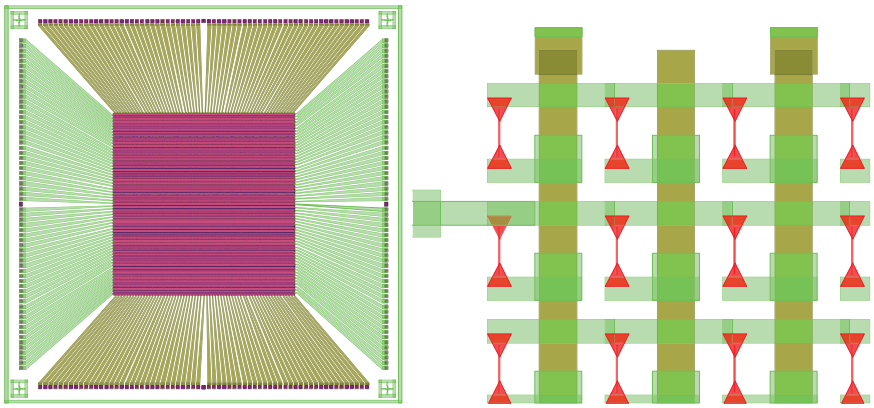

Figure A.8: *Layout of a 128×128 arrays with common source*

A.2. Fabrication process flows

The SiNW fabrication process was mainly described in section 3.1. In this appendix, details of the processing steps were described. The imprint mold was fabricated as described in section 3.1.3

Photolithography masks were fabricated at IBN, the fabrication process need extra 5 masks: Mask 1 for protects the SiNW from the implantation process. Mask 2 for opening the back gate contact. Mask 3 for opening the drain and source contacts. Mask 4 for opening the gate areas of SiNW. Mask 5 for lift-off process.

The process was started with the SOI wafer (SOITEC-USA). The parameter of the SOI wafer was given in table A.1.

Table A.1. Parameters of SOI wafers used in this thesis

Parameters	Top Si layer	Buried oxide	Handle wafer
Crystal orientation	<100>		<100>
Crystal Growth Method	COP free		CZ
Mean thickness	340 ± 20 nm	400 ± 2 nm	
Doping type / species	P type / Boron		P type / Boron
Resistivity	14-22 Ω.cm		14-22 Ω.cm
Flat orientation			<110>

The following table A.2 gives a detail of the fabrication steps and those parameters for the SiNW arrays.

Table A.2. SiNW chips fabrication process flows

steps	Processes	Parameters	comments
Thinned out the SOI wafers and grown oxide hard mask for TMAH			
1	SOI wafer cleaning	Standard RCA processes	Table A.3
2	Wet thermal oxidation	1100°C, 40 min (1st run) 1100°C, 50 min (2st run)	530±5 nm 580±5 nm
3	SiO2 etching	AF-91-1, 10 min HF 1% , 15 min-20 min	 wafers dewet
4	Dry thermal oxide	1000°C, 180 min (1st run) 1000°C, 30 min (2sd run)	100 nm oxide 30 nm oxide
Nanoimprint lithography			
1	Clean wafers and mold	Aceton+isopropanol, 5 min	
2	Resist spin-coating	NX 1020	Table A.4
3	Nanoimprint	Nanonex 2000 120°C / 200 PSI (pre-imprint) 160°C / 450 PSI (main-imprint), 6 min. Demolding temperature: 35°C	Section 3.1.3
4	Residual etching	RIE O_2, 1 min	Section 3.1.3 Table A.5
5	SiO2 hard mask etching	RIE CHF_3, 7 min (1st run) RIE CHF_3, 3 min (2sd run)	Etch-stop was observed by laser interferometer Table A.5
6	Remove resist	RIE O_2, 1 min	
TMAH etching to define SiNW structure			
1	Remove native oxide	HF 1%, 30 sec	Rinsed by water
2	TMAH etching	TMAH 25%, 90°C, 1 min	Rinsed by water

Implantation			
1st run			
1	Removed oxide mask	HF 1%, 22 min	Etch rate 5 nm/min
2	Wafer cleaning	SC0, 10 min	See RCA
3	Oxide mask for implantation	LPCVD:TEOS, 650°C, 100 nm	Rate 3 nm/min
4	Lithography	Mask 1, AZ5214	Table A.6
5	Etch oxide mask	RIE CHF_3, 3 min	
6	Hard beak resist	130°C, 10 min	Hot plate
7	Implantation	B, 7 keV, $1x10^{14}/cm^2$	
8	Remove resist	RIE O_2, 8 min	
9	Remove LPCVD oxide on SiNW	HF 1%, 5 min	Rinsed by water
10	Wafer cleaning	SC0, 10 min	
11	Annealing	Oxidation oven, N_2 atmosphere, 900°C, 30 min	
2sd run			
1	Lithography	AZ5124	
2	Oxide etch	HF 1%, 6 min-8 min	Removed hard mask oxide on the contact line
3	Hard beak resist	130°C, 10 min	Hot plate
4	Implantation	B, 6 keV, $1x10^{15}/cm^2$	
5	Remove resist	RIE, O_2, 1min and then acetone 10 min	
6	Oxide etch	HF 1%, 6min-8 min	Remove oxide on the SiNW
7	Cleaning	RCA standard	
8	Annealing	Oxidation oven, N_2 atmosphere,	

		900°C, 30 min	
LPCVD for passivation layer			
1st run			
1	Cleaning	RCA1	
2	SiO2 for passivation layer	LPCVD: TEOS, 650°C, 300 nm	
2sd run			
1	Cleaning	RCA standard	
2	Dry thermal oxidation	820°C, 40 min	6 nm
3	SiO2 for passivation layer	LPCVD: TEOS, 650°C, 400 nm	
Gate and contact pad opening			
1	Lithography	AZ5214	Mask2+mask3
2	Oxide etch	HF 1%, 10 min	Open gate areas and bond pad
3	Remove resist	Acetone + isopropanol	
4	Lithography	AZ5214	Mask4
5	Oxide etched	AF-91-9, 8 min	Open back-gate contacts through the BOX
6	Remove resist	Acetone-isopropanol	
7	Cleaning wafer	RCA standard	
8.	Gate oxidation	Dry thermal oxidation, 820°C, 45 min	6-7 nm
Metal deposition for contact pads			
1	Lithography	AZ5214	Mask 5
2	Oxide etch	HF 1%, 2 min	Remove the thermal gate oxide on contact pads
3	Metal evaporation	E-beam evaporation, Al: 150 nm, Ti: 10 nm, Au: 150 nm	Si/Al/Ti/Au

4	Lift-off	Acetone, overnight	
5	Annealing	RTP oven, N_2 atmosphere, 400°C, 10 min	*ohmic* contact

Table A.3. Standard RCA recipes for wafer cleaning

Steps	Process	Parameters
1	SC0	H_2O_2:H_2SO_4 = 2:1, 60°C, 10 min
2	HF	1% (v/v) HF, room temperature, 10 seconds
3	SC1	H_2O:H_2O_2:NH_4OH=20:4:1, 60°C, 10 min
4	HF	1% (v/v) HF, room temperature, 10 seconds
5	SC2	H_2O:H_2O_2:HCl=20:1:1, 60°C, 10 min

Table A.4: Recipes for thermal nanoimprint resist coating

Step	Process	Parameters
1	Spin coating	4000 rpm, 30 s
2	Soft bake	90°C,20 min

Table A.5 RIE Program for etching resist and SiO_2

Recipes	Parameter
$RIEO_2$	200W, 20 sccm, 0.02 mbar
$RIECHF_3$	200W, 30 sccm, 0.03 mbar

Table A.6, Recipes for photolithography with AZ5214 resist

Step	Process	Parameter
1	Clean wafer	Acetone, isopropanol, water
2	Dehydrate	180°C, 5 min
3	HMDS coating	Spin-coating, 500 rpm-30 s, 4000rpm–30 s
4	AZ5214 coating	Spin-coating, 500 rpm–30 s, 4000rpm–30 s

5	Soft bake	90°C, 5 min, hot plate
6	Alignment and expose	Suess MA6, 4.7 s, 0.7 W/cm^2
7*	Post expose bake	115°C, 2 min
8*	Flood expose	Suess MA6, 20 s, 0.7 W/cm^2
9	Development	MIF326, 50 s
10	Rinsed	dd water, 10 min

A.3 List of equipment and chemical used in SiNW fabrication.

Table A.7. List of equipment used for chip fabrication

Name	Type	Company
Lithography equipment		
Optical lithography	MA6, 365 nm	Suess
EBL	EBPG 5HR	Leica
Nanoimprinter	NX-2000	Nanonex
Characterization equipment		
Ellipsometer	SE400 Laser	SENTECH
	SE800 spectra	SENTECH
Profilometer	Dektak 3030	Vecco
4 point measurement	AP-150	Vecco
SEM	Gemini 1500 VP	Zeiss
STEM	Titan 80-300	FEI

FIB	Helios NanoLab 400S	FEI
Layer production		
LPCVD	E1200 R&D	Centrotherm
Metal deposition	PLS 500	Pfeiffer
Oxidation oven		Tempress
RTP	AET ADDAX RTP RM	PRIMA
Ion implantation	NV 3204	Eaton
RIE Laser interferometer	 SL 50	Oxford instruments SOFIE instruments
Megasonic		SONOSYS

Table A.8. List of the chemical used for chip fabrication in clean room

Chemical	Company
Resist and development	
AZ5214	Micro chemicals
UV 6.06	Micro resist technology
PMMA AR-P 699.04	Allresist
NXR 1020	Nanonex
AR 600–55	ALLRESIST
ma-D 532	Micro resist techonology
MIF 326	Micro chemicals

Cleaning and wet etching	
Acetone	BASF
Isopropanol	BASF
H_2O_2 (31%)	BASF
HCl (37%)	BASF
H2SO4 (94%)	BASF
NH4OH (25%)	BASF
TMAH (25%)	Riedel-de-Haen
1H,1H,2H,2H-Perfluorooctyltrichlorosilane	Fluka

B. Chemical and buffer solutions use for biomolecular sensing

B.1. Phosphate buffer saline (PBS)

Regent	Concentration
KCl	2.7 mM
NaCl	137 mM
Na_2HPO_4	8.1 mM
KH_2PO_4	1.47 mM

Reagents dissolved in H_2O (bidest). Adjusted to pH 7.4.

0.01 x PBS buffer solution was prepared by diluting 100 times PBS buffer in H_2O.

B.2. Phosphate buffer solution for DNA immobilization

	Regent	Concentration
Solution A	Na_2HPO_4	150 mM
Solution B	NaH_2PO_4	150 mM

Phosphate buffer solution was prepared by mixing two solutions to reach the respective pH 8.5

B.3. DNA sequence

DNA was purchased for MWG-Biotech Ag, Germany.

Name	sequence
ssDNA	amino C6-5'-ATGAACACTGCATGTAGTCA-3'
cDNA	5'-TGACTACATGCAGTGTTCAT-3'
fluorescence cDNA	Cy3-5'-TGACTACATGCAGTGTTCAT-3'

B.4. List of chemicals

If not stated otherwise, all chemicals were purchased from Sigma (Sigma-Aldrich Chemie GmbH, Taufkirchen, Germany).

Titrisol buffer PH 1-14	Merck, KGaA
KH_2PO_4	Carl Roth GmbH
Na_2HPO_4	Carl Roth GmbH
NaH_2PO_4	Carl Roth GmbH
Biotin	Pierce Biotechnology, Inc., USA
Hellmanex	Hellmanex

C. Abbreviations

AC	Alternative current
APTES	3-aminopropyl-triethoxysilane
BOX	Buried oxide
BG	Back gate

CMOS	Complementary metal oxide semiconductor
COP	Crystal originating particles
CVD	Chemical vapor deposition
CZ	Czochralski
D	Drain
DIC	Differential Interference Contrast
DNA	Deoxyribonucleic acid
ssDNA	Single-stranded Deoxyribonucleic acid
cDNA	Complementary Deoxyribonucleic acid
DUV	Deep UV lithography
EBL	electron-beam lithography
EIS	Electrolyte-insulator-semiconductor
FET	Field-effect transistor
FIB	Focused Ion Beam
FG	Front gate
G	Gate
GPTES	3-glycidoxypropyltrimethoxysilane
IBN	Institute of Nano- and Biosystems
ISFET	Ion sensitive field-effect transistor
LCC	Ceramic Leadless Chip Carrier
LPCVD	Low pressure chemical vapor deposition
M	Molar/liter
MEA	Micro electrode array
MOSFET	Metal oxide semiconductor field-effect transistor
MOS	Metal oxide semiconductor
NIL	Nanoimprint lithography

NW	Nanowire
ONO	Oxide-nitride-oxide
PBS	Phosphate Buffered Saline
PDL	Poly(D)lysine
PDMS	Polydimethylsiloxane
PCB	Printed circuit board
PE	Polyelectrolytes
PAH	Poly (allylamine hydrochloride)
PSS	Poly(sodium 4-styrensulfonate)
PMMA	Polymethylmethacrylat
PNA	Peptide nucleic acid
RCA	Wafer cleaning recipes of Radio Corporation of America
RE	Reference electrode
RIE	Reactive ion etching
rpm	Round per minute
RTP	Rapid Thermal Processing
S	Source
SiNW	Silicon nanowire
SEM	Scanning electron microscope
SMU	source measurement units
SNAP	superlattice nanowire pattern transfer
SOI	Silicon-on-Insulator
SSC	Saline-sodium citrate buffer
STEM	Scanning transmission electron microscope
USB	Universal serial bus
TMAH	Tetramethylamoniumhydroxid

VLS	Vapor-liquid-solid method

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